1. Features and benefits

- Motor driver
  - Driver for DC/BLDC/Stepper motor
  - Ron=0.8Ω typ. for 1 half-bridge + shunt
  - 2x NFET for each half-bridge
  - on-chip charge-pump for top-NFETs
  - V_{ds} protection for all NFETs
- Microcontroller:
  - 2x MLX16-FX, application CPU + CoProcessor
  - MLX4, communication CPU
  - 2x watch-dog
  - +50 input interrupt controller
  - Common purpose timer
- Memories split per CPU
  - 2x MLX16-FX memories:
    - 32/64 kByte Flash with ECC
    - 10 kByte ROM
    - 2/4 + 3 kByte RAM
    - 512 Byte EEPROM with ECC
  - MLX4 memories:
    - 6 kByte ROM
    - 512 Byte RAM
- Pin-compatible drivers in SO8 and QFN24
  - MLX81350 < 0.5A
  - MLX81352 < 1A
  - MLX81354 < 1A, 64KB Flash
- Gen4 MLX81350/52/54 is compatible with Gen3 MLX81330/32/34
- Periphery
  - Configurable RC-clock 24..40 MHz
  - 8x general purpose IO's, digital, analog, 1x high-voltage input, UART, SPI, I2C-Master & Slave, AB(I)
  - 5x 16-bit motor PWM timers
  - 2x 16-bit timers
  - 13-bit differential ADC with < 1.2 µs conversion time with multiple channels
  - Differential current sense amplifier
  - Temperature sensor, over-temperature detection
  - Over-current detection, over-voltage and under-voltage protection
- Voltage regulators
  - Internal voltage regulators, directly powered from 12V battery supply
  - Operating voltage Vs = 5.5V to 28V
  - Operation down to 3.5V with reduced analog characteristics, down to 3V without losing register content, down to 1.5V with intact RAM memory
  - Low standby current consumption of typ 25µA (max 50 µA) in sleep mode
  - Wake-up possible via LIN, external pins or internal wake-up timer
- Bus interface
  - LIN 2.x/SAE J2602 and ISO17987-4 compliant LIN slave
- **Automotive AEC-Q100 qualified**

2. Application examples

- Small Stepper/BLDC flap or valve, up to 1A per phase
- Small DC flap/valve, or single-coil fan/pump, up to 1.4A

3. Ordering information

Order Code	Temp. Range	Package	Delivery	Remark
MLX81352 LLW-BMX-202-RE	-40 - 150 °C	QFN24_WF 4x4	Reel	With 8x IO, 32kB Flash
MLX81352 LDC-BMX-202-RE	-40 - 150 °C	SO8-ep	Reel	Stepper with 1x IO, 32kB Flash
MLX81354 LLW-BMX-202-RE	-40 - 150 °C	QFN24_WF 4x4	Reel	With 8x IO, 64kB Flash
MLX81354 LDC-BMX-202-RE	-40 - 150 °C	SO8-ep	Reel	Stepper with 1x IO, 64kB Flash

Table 1 – Ordering information

4. Family Concept

	MLX81350	MLX81352	MLX81354
MCU Memory	32 KB Flash + 16 KB ROM	**32 KB Flash + 16 KB ROM**	**64 KB Flash + 16 KB ROM**
MCU EEPROM	64x 8 Byte	**64x 8 Byte**	**64x 8 Byte**
MCU RAM	2.5 KB	**2.5 KB**	**4.5 KB**
CoProcessor + 3kB RAM	Yes	**Yes**	**Yes**
Driver	4x Driver on-chip typ. 3Ω Halfbridge	**4x Driver on-chip typ. 0.8Ω Halfbridge**	**4x Driver on-chip typ. 0.8Ω Halfbridge**
IO pins (analog, digital)	3x LV + 1x HV/LV	**7x LV + 1x HV/LV**	**7x LV + 1x HV/LV**
Motor current sense	Low side, On-chip	**Low side, On-chip**	**Low side, On-chip**
ADC for current, voltage, external sensors	13-bit differential 1µs update rate	**13-bit differential 1µs update rate**	**13-bit differential 1µs update rate**
Sensor interface (3V/5V supply)	analog, pwm, spi, sent, I^2C, uart	**analog, pwm, spi, sent, I2C, uart, AB(I)**	**analog, pwm, spi, sent, I^2C, uart, AB(I)**
Sensorless support (hw + sw)	Yes	**Yes**	**Yes**
LIN auto-address support (AA)	Yes	**Yes**	**Yes**
Maximum IC Temperature (with validated mission profile)	T_j = 175°C	**Tj = 175°C**	**Tj = 175°C**
Package	SO8-ep QFN24, 4x4	**SO8-ep QFN24,4x4**	**SO8-ep QFN24,4x4**

Table 2 – Family Overview

5. Revision history

Version	Date	Description of changes
Rev 001	19/11/2026	MLX81352/54 product abstract, initial version

Table 3 – Revision history

6. Contents

1. Features and benefits 1
2. Application examples 1
3. Ordering information 2
4. Family Concept 2
5. Revision history 3
6. Contents 4
7. IC block diagram 5
8. Technical description 6
8.1. Package data QFN24 6
8.2. Package data SOIC8-EP 7
8.3. Package pin-out 8
8.4. Package marking 11
9. Typical application schematic 12
10. Electrical characteristics 13
10.1. Absolute maximum ratings 13
10.2. Operating range 14
10.3. Electrical specifications 15
10.3.1. Current consumption 15
10.3.2. Supply system 15
10.3.3. Clock generation 18
10.3.4. Motor driver module 18
10.3.5. VSM supply sensor 20
10.3.6. Over-temperature detection 20
10.3.7. Off-State Diagnostics (OSD) 20
10.3.8. ADC 21
10.3.9. IO 22
10.3.10. LIN 23
11. Disclaimer 26

7. IC block diagram

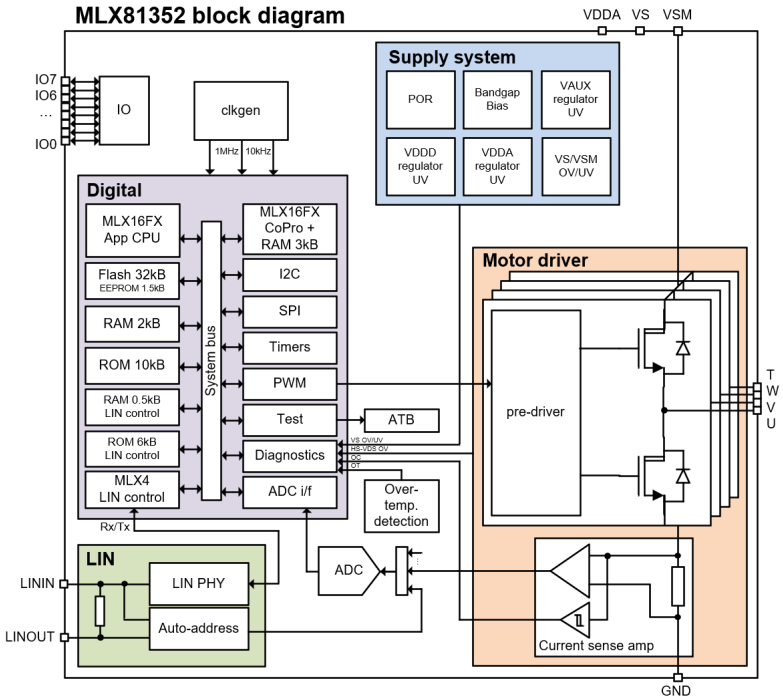


Figure 1 – IC Block diagram MLX81352

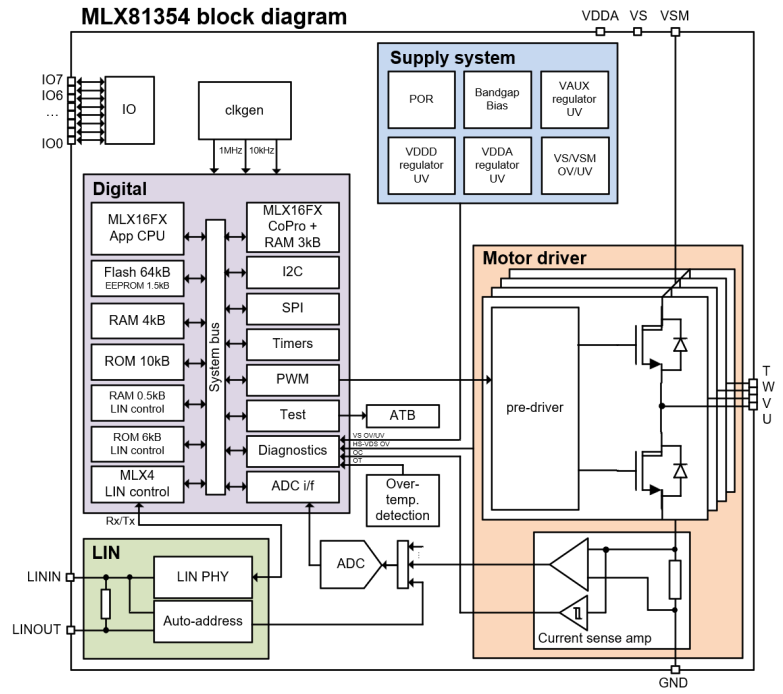
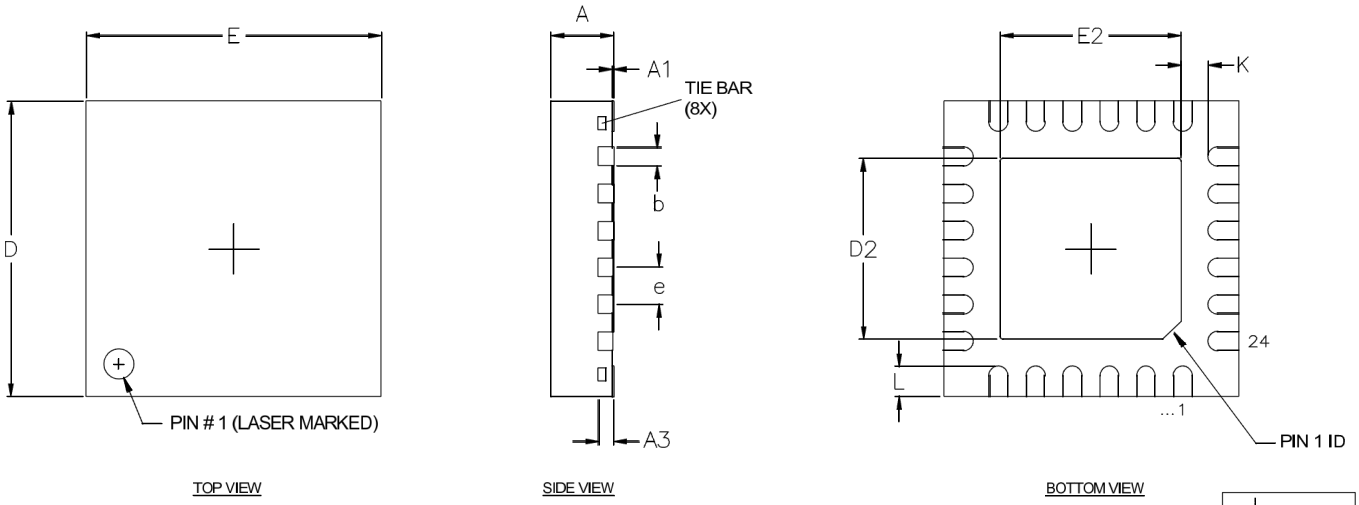


Figure 2 – IC block diagram MLX81354

Note : Some pins are not available in SOIC8-ep production versions. All pins are available in QFN24 production version.

8. Technical description

8.1. Package data QFN24

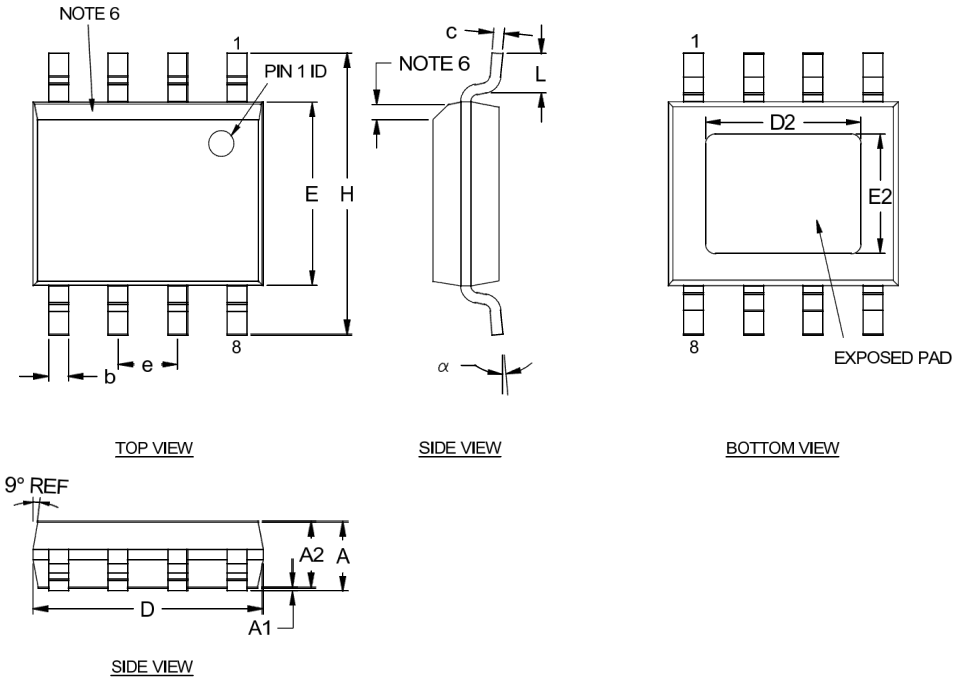


SYMBOL	ALL DIMENSION ARE IN MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.35	2.45	2.55
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
K	0.20	---	---
b	0.18	0.25	0.30
e		0.50 BSC	

NOTE :
1. EXPOSED TIE BAR SHOULD BE KEPT FREE FROM SOLDER.
2. (OPTIONAL) SIDE WALL IMMERSION TIN PLATING MIN 1um THICK.

Figure 3 – Package data QFN24

8.2. Package data SOIC8-EP



SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	1.40	---	1.68
A1	0.00	---	0.13
A2	1.37	---	1.58
D	4.80	4.90	5.00
E	3.81	3.90	3.99
D2	3.00	3.30	3.55
E2	2.29	2.50	2.79
H	5.80	6.00	6.20
L	0.41	---	1.27
b	0.36	0.41	0.46
c	0.19	---	0.25
e	1.27 BSC		
α	0°	---	8°

NOTE :
1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS OF MAX 0.15 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTERLEADS FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.10 mm.
5. LEAD TO LEAD COPLANARITY MAX 0.100 mm.
6. MOLD CHAMFER ANGLE CAN DIFFER. DEPENDING ON MOLD TOOLING IT IS POSSIBLE TO HAVE NO CHAMFER OR A 45 DEGREE CHAMFER WITH TYPICAL WIDTH OF 0.33 mm. CONTACT MELEXIS IN CASE OF QUESTIONS.
7. DAMBAR CUT PORTION AT THE LEAD SHOULDER CAN HAVE TRACES OF EXPOSED COPPER. CONTACT MELEXIS IN CASE OF QUESTIONS.

Figure 4 – Package Drawing SOIC8 with exposed pad

8.3. Package pin-out

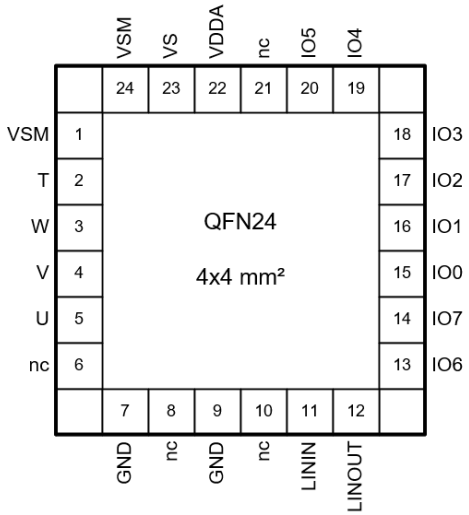


Figure 5 – Pin-out diagram QFN24

SO8-ep package variants to optimize system BOM, PCB wiring and solution cost, are available on request for high-volume applications >5M/yr.

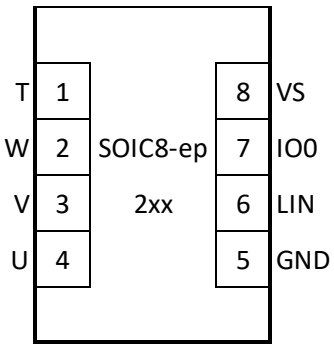


Figure 6 – Pin-out diagram SO8-ep, -2xx variant (Stepper motor, 1x IO)

#	Pin name	Description
QFN24, 4x4mm		**All pins accessible**
1	VSM	Supply voltage for motor driver
2	T	T-phase
3	W	W-phase
4	V	V-phase
5	U	U-phase
6	nc	
7	GND	Ground
8	nc	
9	GND	Ground
10	nc	
11	LIN-IN	LIN input
12	LIN-OUT	LIN output (for auto-addressing)
13	IO6	LVIO + test input for development
14	IO7	LVIO + test output for development
15	IO0	LVIO + HVI (high-voltage input)
16	IO1	LVIO
17	IO2	LVIO
18	IO3	LVIO
19	IO4	LVIO
20	IO5	LVIO
21	nc	
22	VDDA	3.3V/5V analog supply voltage
23	VS	Supply voltage for MCU
24	VSM	Supply voltage for motor driver

Table 4 – Pin-out description for QFN24

SO8-ep		8-pins accessible (201 variant)
1	T	T-phase
2	W	W-phase
3	V	V-phase
4	U	U-phase
5	GND	Ground
6	LIN	LIN input
7	IO0	LVIO + HVI (high-voltage input)
8	VS	Supply voltage (MCU + Driver)

Table 5 – Pin-out description for SO8-ep, -2xx variant (Stepper motor, 1x IO)

8.4. Package marking

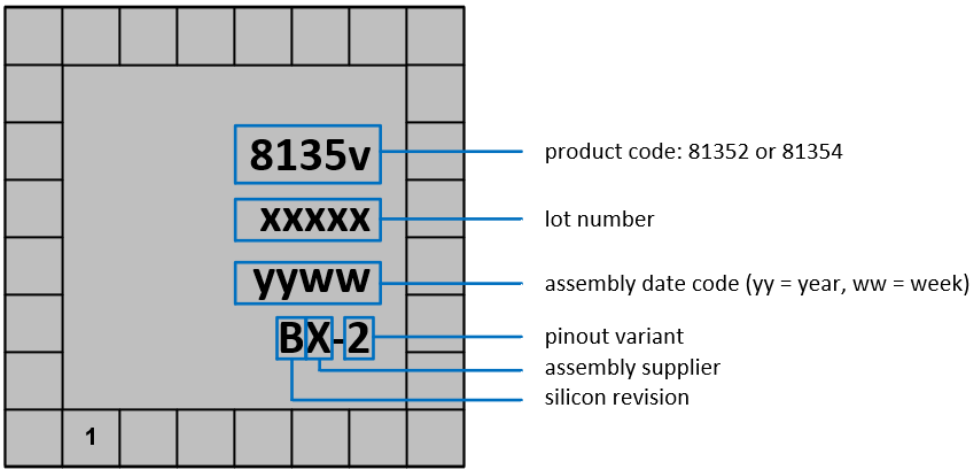


Figure 7 – Package Marking QFN24

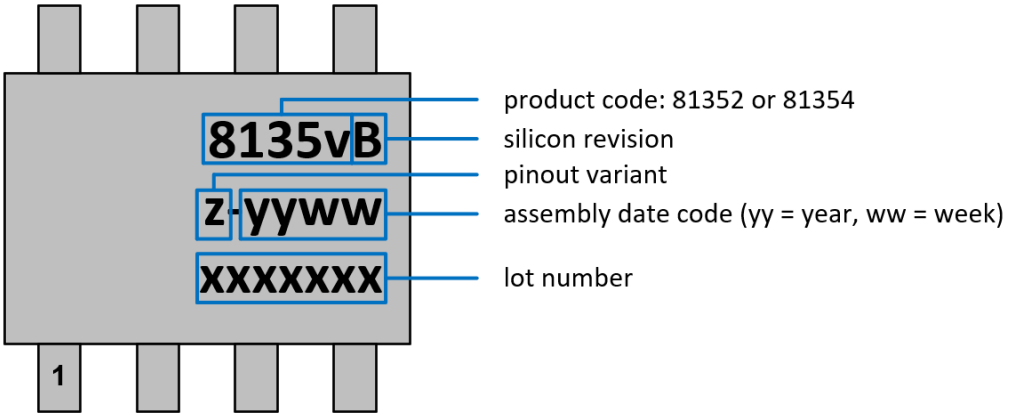


Figure 8 – Package Marking SOIC8-EP

9. Typical application schematic

In the following schematic examples, external components are indicated that may be needed to protect the IC against EMC / ESD pulses. Depending on ECU conditioned power, overvoltage and reverse polarity discretes may not be needed. Capacitor discretes or capacitor values will depend on specific OEM ESD/EMC requirements, see chapters **Error! Reference source not found.** and **Error! Reference source not found.**.

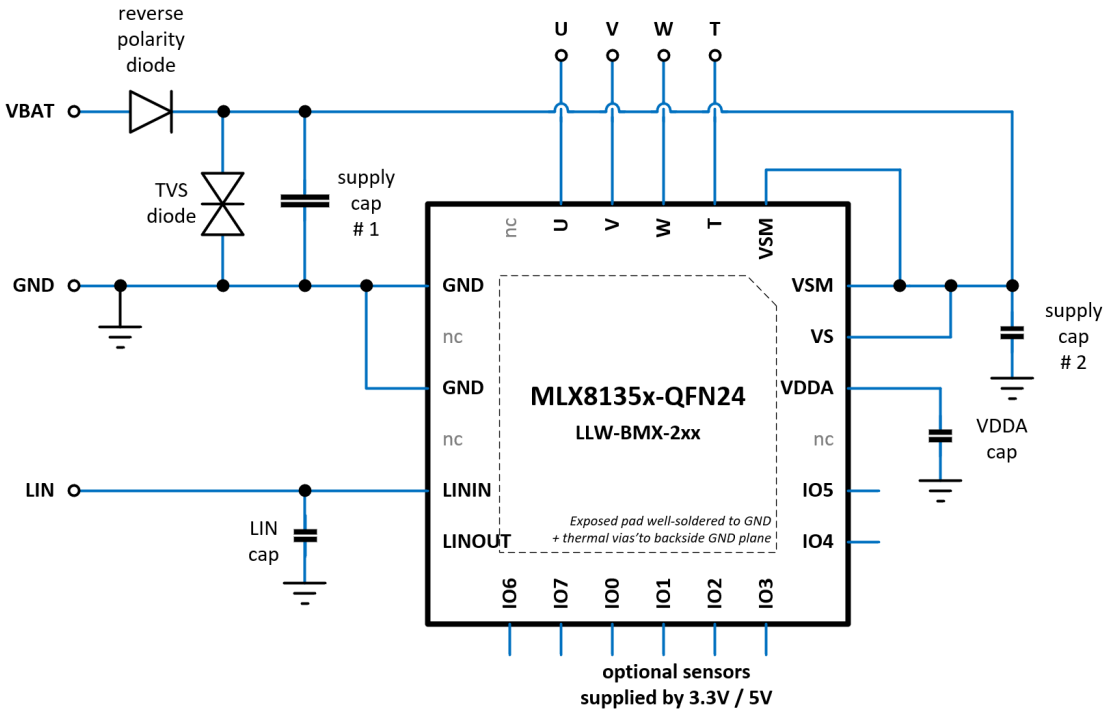


Figure 9 – Typical stepper/BLDC/DC motor schematic with MLX81352/54 in QFN24

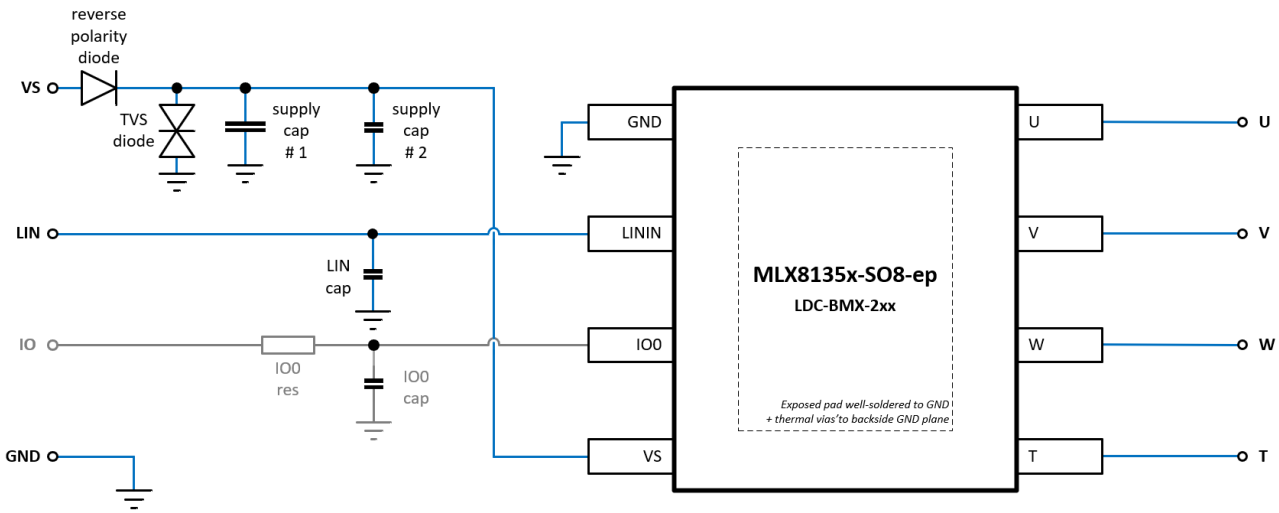


Figure 10 – Typical stepper/BLDC/DC motor schematic with MLX81352/54 in SO8-ep, -2xx variant

10. Electrical characteristics

10.1. Absolute maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage	VS, VSM	-0.3		28	V	
Supply voltage	VS, VSM	-0.3		40	V	t < 500ms
Supply voltage transient	VS.tr1	-100			V	ISO 7637-2 pulse 1 [1]
Supply voltage transient	VS.tr2			75	V	ISO 7637-2 pulse 2 [1]
Supply voltage transient	VS.tr3	-150		100	V	ISO 7637-2 pulses 3a, 3b [1]
Output voltage	VDDA	-0.3		5.5	V	
LIN bus voltage	VLIN	-40			V	Referenced to VS
LIN bus voltage	VLIN			40	V	Referenced to GND
LIN bus voltage transient	VLIN.tr1	-30			V	ISO 7637-3 DCC slow – [2]
LIN bus voltage transient	VLIN.tr2			30	V	ISO 7637-3 DCC slow + [2]
LIN bus voltage transient	VLIN.tr3	-150		100	V	ISO 7637-2 pulses 3a, 3b [2]
Phase pin voltage	VAN_PH	-0.3		VSM+0.3	V	U, V, W, T
Analog HV voltage	VAN_HV	-0.3		VS+0.3	V	IO0 (HV input mode)
Analog LV voltage	VAN_LV	-0.3		VDDA+0.3	V	IO0, IO1, IO2, IO3
Digital input voltage	VIN_DIG	-0.3		VDDA+0.3	V	IO0, IO1, IO2, IO3
Digital output voltage	VOUT_DIG	-0.3		VDDA+0.3	V	IO0, IO1, IO2, IO3
ESD HBM capability	ESD_HBM	-2		2	kV	All pins except LININ, LINOUT
ESD HBM capability	ESD_HBM_LIN	-6		6	kV	Pins LININ, LINOUT
ESD CDM capability	ESD_CDM	-500		500	V	All pins
Junction temperature	TJ	-55		175	ºC	
Thermal resistance, junction - ambient	RTH_JA		48		K/W	In free air, QFN24 package [3]

Thermal resistance, junction - case	RTH_JC		7		K/W	QFN24 package [3]
Thermal resistance, junction - ambient	RTH_JA		48		K/W	In free air, SOIC8-EP package [3]
Thermal resistance, junction - case	RTH_JC		7		K/W	SOIC8-EP package [3]

Table 6 – Absolute maximum ratings

[1] ISO 7637 test pulses are applied to VS via a reverse polarity diode and blocking capacitor.
[2] ISO 7637 test pulses are applied to LIN via a coupling capacitance of 1nF.
[3] Valid for low thermal conductivity board (JEDEC).

10.2. Operating range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage	VS, VSM	6.5	12	28	V	Driver full performance
Supply voltage	VS, VSM	5.5		6.5	V	Driver reduced performance [1]
Supply voltage	VS	4		28	V	Analog full performance [2]
Supply voltage	VS	3.5		4	V	Analog reduced performance [3]
Supply voltage	VS	3		28	V	Digital functional
Supply voltage	VS	1.5		28	V	SRAM content valid
Junction temperature	TJ	-40		150	ºC	Limited time at Tj=175 ºC [4]

Table 7 – Operating range

[1] Motor driver is functional at reduced performance (higher bridge resistance, reduced accuracy of current sense amplifier)
[2] For 5V VDDA operation, the minimum voltage for full performance increases to 6V.
[3] 3.3V regulator is functional at reduced performance (lower current capability)
[4] Extended temperature range with Tj=175 ºC is only allowed for a limited time, customer's mission profile has to be agreed by Melexis as an obligatory part of the Part Submission Warrant (PSW).

10.3. Electrical specifications

10.3.1. Current consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Normal working current	INOM		10	15	mA	
Sleep mode current	ISLEEP		25	50	µA	VS=28V,Tj=85degC
Stop mode current	ISTOP		250	500	µA	VS=28V,Tj=85degC
Holding mode current	IHOLD		5	7	mA	

Table 8 – Electrical specifications: current consumption

10.3.2. Supply system

10.3.2.1. VDDA 3.3V regulator (5V option, external C: 0 … 330nF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
3.3V analog supply voltage (default)	VDDA	3.2	3.3	3.4	V	Bandgap and VDDA regulator trimmed
3.3V external current capability	IVDDA_EXT	0		15	mA	VS >= 4V
3.3V under-voltage detection threshold	VTH_UV_VDDA	2.75	2.85	2.95	V	VDDA ramping down
3.3V under-voltage detection hysteresis	VHY_UV_VDDA	0.1	0.15		V	
5V option (SWITCH_VDDA_TO_5V=1)						
5V analog supply voltage (option)	VDDA	4.85	5	5.15	V	Bandgap and VDDA regulator trimmed
5V external current capability	IVDDA_EXT	0		15	mA	VS >= 6V
5V under-voltage detection threshold	VTH_UV_VDDA	3.95	4.1	4.25	V	VDDA ramping down
5V under-voltage detection hysteresis	VHY_UV_VDDA	0.1	0.15		V	

Table 9 – Electrical specifications: VDDA regulator

10.3.2.2. VSM under-voltage and over-voltage detection

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VSM under-voltage detection threshold	VTL_UV_VSM	3.5	4	4.5	V	PRUV_VSM=0
VSM under-voltage detection threshold	VTL_UV_VSM	4.5	5	5.5	V	PRUV_VSM=1
VSM under-voltage detection threshold	VTL_UV_VSM	5.5	6	6.5	V	PRUV_VSM=2
VSM under-voltage detection threshold	VTL_UV_VSM	6.5	7	7.5	V	PRUV_VSM=3
VSM under-voltage detection threshold	VTL_UV_VSM	7.5	8	8.5	V	PRUV_VSM=4
VSM under-voltage detection threshold	VTL_UV_VSM	8.5	9	9.5	V	PRUV_VSM=5
VSM under-voltage detection hysteresis	VHY_UV_VSM	0.1	0.5	1	V	
VSM over-voltage detection threshold	VTH_OV_VSM	20	22	24	V	PROV_VSM=0
VSM over-voltage detection threshold	VTH_OV_VSM	22	24	26	V	PROV_VSM=1
VSM over-voltage detection threshold	VTH_OV_VSM	38	40	42	V	PROV_VSM=2
VSM over-voltage detection hysteresis	VHY_OV_VSM	1	2	3	V	

Table 10 – Electrical specifications: VSM over- and under-voltage detection

10.3.2.3. VS under-voltage detection

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VS under-voltage detection threshold	VTL_UV_VS	3.5	4	4.5	V	PRUV_VS=0
VS under-voltage detection threshold	VTL_UV_VS	4.5	5	5.5	V	PRUV_VS=1
VS under-voltage detection threshold	VTL_UV_VS	5.5	6	6.5	V	PRUV_VS=2
VS under-voltage detection threshold	VTL_UV_VS	6.5	7	7.5	V	PRUV_VS=3
VS under-voltage detection threshold	VTL_UV_VS	7.5	8	8.5	V	PRUV_VS=4
VS under-voltage detection threshold	VTL_UV_VS	8.5	9	9.5	V	PRUV_VS=5
VS under-voltage detection hysteresis	VHY_UV_VS	0.1	0.5	1	V	

Table 11 – Electrical specifications: VS under-voltage detection

10.3.2.4. Wake-up circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Wake-up filter time IO pins	TFILT_WU_IO	15		80	µs	
Wake-up filter time LIN pin	TFILT_WU_LIN	28		125	µs	
Wake-up time internal timer	TWU_INT		n/a			WUI=00 (no wake-up)
Wake-up time internal timer	TWU_INT		4096 / FOSC_10K			WUI=01 (~0.4 s)
Wake-up time internal timer	TWU_INT		8192 / FOSC_10K			WUI=10 (~0.8 s)
Wake-up time internal timer	TWU_INT		16384 / FOSC_10K			WUI=11 (~1.6 s)

Table 12 – Electrical specifications: wake-up circuit

10.3.3. Clock generation

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency 1MHz oscillator	FOSC_1M	-5%	1	+5%	MHz	Trimmed
Frequency Main Oscillator (MCU_CLK) – 24MHz	FHFO_24M	-5%	24	+5%	MHz	Trimmed
Frequency Main Oscillator (MCU_CLK) – 28MHz	FHFO_28M	-5%	28	+5%	MHz	Trimmed
Frequency Main Oscillator (MCU_CLK) – 32MHz	FHFO_32M	-5%	32	+5%	MHz	Trimmed (**default setting**)
Frequency Main Oscillator (MCU_CLK) – 36MHz	FHFO_36M	-5%	36	+5%	MHz	Trimmed
Frequency Main Oscillator (MCU_CLK) – 40MHz	FHFO_40M	-5%	40	+5%	MHz	Trimmed
Frequency 10kHz oscillator	FOSC_10K	5	10	20	kHz	
Timing accuracy	TIMING_ACC	-1.5%		1.5%	%	Timing accuracy after sw correction using EEPROM calibration values [1]

Table 13 – Electrical specifications: clock generation

[1] Improved timing accuracy through EEPROM calibration values is only valid for frequencies 28MHz, 32MHz, 36MHz and 40MHz.

10.3.4. Motor driver module

10.3.4.1. **Charge pump clock**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Charge pump clock frequency	FOSC_CP	58	60	62	MHz	Trimmed
Charge pump clock frequency	FOSC_CP	80	82	84	MHz	Trimmed (**default setting** [1])

Table 14 – Electrical specifications: driver clock

[1] Chargepump default setting when MLX SW platform is used.

10.3.4.2. **Output stage**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Half-bridge phase current	IHB			1.0	Apk	During normal operation
Half-bridge phase current	IHB			0.7	Arms	During normal operation
Half-bridge phase boost current	IHB			1.3	A	< 1s, ambient temperature -40°C…85°C [2]
2x half-bridge phase boost current	IHB			1.8	A	< 1s, ambient temperature -40°C…85°C, 2 phases in parallel [2]
Half-bridge resistance	RHB		0.8	1.6	Ω	TopFET + BottomFet + Shunt
Duty cycle range of PWM output	DC_OUT	2		98	%	For switching 20KHz PWM (0% or 100% can be set as well)
Duty cycle of PWM output	DC_OUT	1		3	%	20KHz PWM PWM duty cycle setting = 2%
Duty cycle of PWM output	DC_OUT	97		99	%	20KHz PWM PWM duty cycle setting = 98%
FET over-current detection threshold	ITH_DS_HS	1.6	2.2	2.8	A	

Table 15 – Electrical specifications: output stage

[2] Time between boost cycles is 2x boost time.

10.3.4.3. **Current sense amplifier**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Sense resistor	RCS		0.1		Ω	
Input range	ICS	-2		2	A	Measurable range by 13-bit ADC
Over-current detection threshold	ITH_OC	0		3	A	Adjustable through 8bit DAC
Gain	GCS	-5%	0.75	5%	V/A	Trimmed and calibrated (0.54 mA/lsb)
Over-current detection threshold accuracy	ITH_OC	-10		10	%	OCD threshold = 2A

Table 16 – Electrical specifications: current sense amplifier

10.3.5. VSM supply sensor

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Voltage range for ADC measurement				32	V	Measurement of VSM/20
VSM filter cut-off frequency				4	kHz	

Table 17 – Electrical specifications: VSM supply sensor

10.3.6. Over-temperature detection

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
OTD threshold	TTH_OT	175	185	195	ºC	Temperature ramping up
OTD threshold	TTH_OT	150	160	170	ºC	Temperature ramping down
OTD hysteresis	THY_OT	10	25		ºC	

Table 18 – Electrical specifications: over-temperature detection

10.3.7. Off-State Diagnostics (OSD)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
OSD current source	I_OSD	60	100	200	µA	
OSD voltage	V_OSD	2.55		3.3	V	V_OSD is the voltage on the OSD resistor when sourced with I_OSD.

Table 19 – Electrical specifications – off-state diagnostics (OSD)

10.3.8. ADC

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Reference voltage	VREF_ADC	1.63	1.65	1.67	V	Trimmed and calibrated
Resolution			13		bit	13-bit differential input, includes 1 bit for sign
Sample & Hold time				1	µs	
Conversion time	TCONV			1.2	µs	
DNL		-1		1	LSB	
INL		-3		3	LSB	
ADC channel accuracy - 3.3V LV channels with 1/2.2 divider)		-30		30	mV	0V – 3.3V input, calibrated acc. calibration document
ADC channel accuracy - 5V LV channels with 1/3.3 divider		-45		45	mV	0V – 5V input, calibrated acc. calibration document
ADC channel accuracy – HV channels with 1/20 divider		-0.20		0.20	V	< 5V input, calibrated acc. calibration document
ADC channel accuracy - HV channels with 1/20 divider		-0.40		0.40	V	<32V input, calibrated acc. calibration document
ADC channel accuracy - VSMF channel with 1/20 divider		-0.20		0.20	V	<20V input, calibrated acc. calibration document 0C-85C Temp.range, TBC by post-solder analysis, or customer calib.
ADC channel accuracy - VSMF channel with 1/20 divider		-0.33		0.33	V	20V-32V input, calibrated acc. calibration document 0C-85C Temp.range, TBC by post-solder analysis, or customer calib.
ADC temperature channel accuracy		-10		10	ºC	Calibrated acc. calibration document
ADC channel selection		0		28		See **Error! Reference source not found.**

Table 20 – Electrical specifications : ADC

10.3.9. IO

Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
Input threshold level L → H				2.4	V	VDDA = 3.3V
Input threshold level H → L		1			V	VDDA = 3.3V, [1]
Input threshold level L → H				3.5	V	VDDA = 5V
Input threshold level H → L		1.5				VDDA = 5V, [1]
Input hysteresis		0.1			V	
Output voltage L, IO1…7				0.4	V	ILOAD = 3mA
Output voltage L, IO0				0.4	V	ILOAD = 3mA
Output voltage H, IO1…7		VDDA - 0.4V			V	ILOAD = 3mA
Output voltage H, IO0		VDDA - 0.5V			V	ILOAD = 3mA, VS > 5.5V [2]
Input voltage range for high-voltage ADC measurement		0		32	V	IO0 Measurement of IO0/20
Input voltage range for VDDA=3.3V low-voltage ADC measurement		0		3.5	V	IO0…7 Measurement of IOx/2.2
Input voltage range for VDDA=5V low-voltage ADC measurement		0		5.3	V	IO0…7 Measurement of IOx/3.3

Table 21 – Electrical specifications: IO (some IO's are not available in SO8-ep production version)

[1] If IO0 is used as a global pin, then a series resistor of min. 800Ω / max. 10kΩ needs to be applied.
[2] Value for 3.3V VDDA operation. For 5V VDDA operation, VS > 7V to reach the IO0 high output specification.

10.3.10. LIN

10.3.10.1. LIN transceiver- static

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Transmitter internal capacitance [1]	CLIN		30	40	pF	Response on 14V pulse via 1K
Bus short circuit current	IBUS_LIM	40	100	200	mA	VLIN = VS = 27V, VTxD = 0V
Pull up resistance bus, untrimmed	RSLAVE	20	35	60	kΩ	VDISTERM = 0
Pull up current bus, sleep mode	ISLAVE_SLEEP	-50	-20	-5	µA	VLIN = 0V, VSBY = VAUX, VEN =0
Dominant input leakage current including pull up resistor	IBUS_PAS_dom	-600			µA	VLIN =0V, VS =12V, VTxD = VDDD, VDISTERM = 0 VEN = VDDD, VSBY = 0
Recessive input leakage current	IBUS_PAS_rec		0.25	1	µA	VEN = VDDD, VSBY = 0, VTxD = VDDD, VLIN > VS, 5.5V < VLIN < 27V
Bus reverse current loss of battery [2]	IBUS_NO_BAT		0.25	1	µA	VS = 0V, 0V < VLIN < 27V
Bus current during loss of ground [2]	IBUS_NO_GND	-23		1	µA	VS = VGND = 12V, 0 < VLIN < 27V
Transmitter dominant output voltage [2]	VolBUS	0		0.2×VS	V	Rload = 500Ω
Transmitter recessive output voltage [2]	VohBUS	0.8×VS		1×VS	V	VEN = VDDD, VSBY = 0, VTxD = VDDD or sleep mode
Receiver dominant voltage	VBUSdom			0.4×VS	V	
Receiver recessive voltage	VBUSrec	0.6×VS			V	
Center point of receiver threshold	VBUS_CNT	0.475×VS	0.5×VS	0.525×VS	V	VBUS_cnt=(Vth_dom+Vth_rec)/2
Receiver hysteresis	VHYS			0.175×VS	V	VHYS=(Vth_rec–Vth_dom)

Table 22 – Electrical specifications: LIN transceiver – static

[1] No production test, guaranteed by design and qualification
[2] In accordance to SAE J2602

10.3.10.2. LIN transceiver – dynamic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Propagation delay receiver [1]	trx_pdf			6	µs	CRxD =25pF falling edge
Propagation delay receiver [1]	trx_pdr			6	µs	CRxD =25pF rising edge
Propagation delay receiver symmetry	trx_sym	-2		2	µs	Calculate trx_pdf - trx_pdr
Receiver debounce time [2]	trx_deb	0.5		4	µs	LIN rising & falling edge
LIN duty cycle 1 [2] [3] [5]	D1	0.396				20kbps operation, normal mode Vs = 7 to 18V
LIN duty cycle 2 [2] [3] [5]	D2			0.581		20kbps operation, normal mode Vs = 7 to 18V
LIN duty cycle 3 [2] [3] [5]	D3	0.417				10.4kbs operation, low speed mode Vs = 7 to 18V
LIN duty cycle 4 [2] [3] [5]	D4			0.590		10.4kbs operation, low speed mode Vs = 7 to 18V
tREC(MAX) – tDOM(MIN) [4] [5]	Δt3			15.9	µs	10.4kbs operation, low speed mode
tDOM(MAX) – tREC(MIN) [4] [5]	Δt4			17.28	µs	10.4kbs operation, low speed mode
Slew rate on pin LIN normal mode, untrimmed			1.7		V/ µs	dV/dt between duty cycle measurement points, Vs=12V
Slew rate on pin LIN low speed mode, untrimmed			0.85		V/ µs	dV/dt between duty cycle measurement points, Vs=12V
TxD dominant timeout [6]	ttxd_to		15		ms	Normal mode, vTxD = 0V

Table 23 – Electrical specifications: LIN transceiver – dynamic

[1] This parameter is tested by applying a square wave signal to the LIN. The minimum slew rate for the LIN rising and falling edges is 50V/us
[2] See Figure 11
[3] Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal master termination disabled
[4] In accordance to SAE J2602, see Figure 12
[5] For supply voltage ranges Vs=5.5…7V and Vs=18…27V parametric deviations are possible (target specification is w/o deviations & ppK>2.0)
[6] Parameter in relation to internal signal TxD

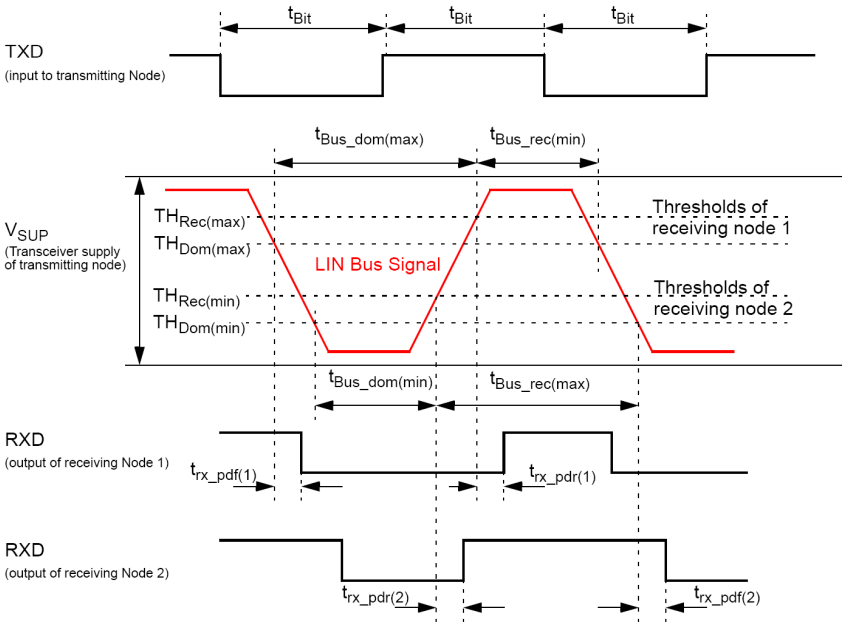


Figure 11 – LIN timing diagram (reference LIN2.1 specification)

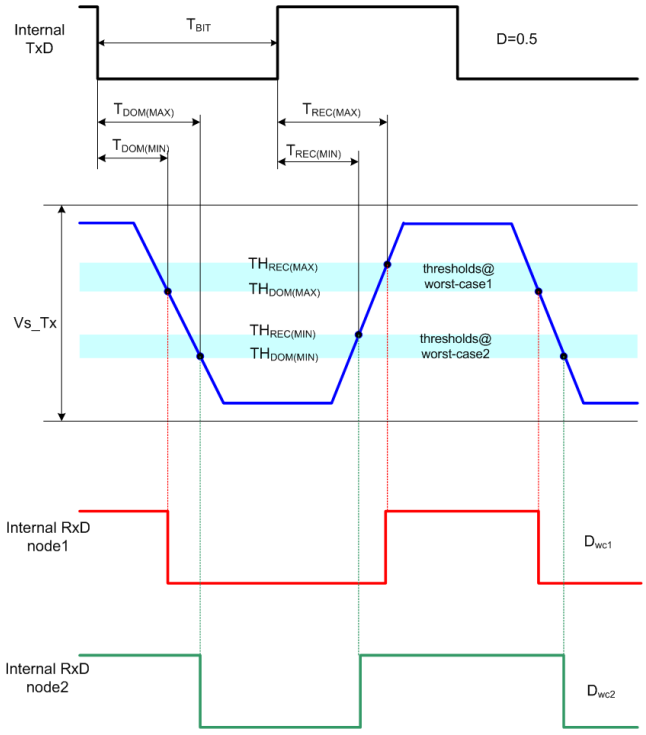


Figure 12 – LIN timing diagram, relation between propagation delay and duty cycle (reference SAE J2602 specification)

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