1. Features and Benefits

- Motor driver
  - 3x PreDriver for DC or BLDC motor
  - Up to 200nC NFETs (12V-48V supply)
    - 0.7 A_{pk} typ. charge current
    - 1.5 A_{pk} typ. discharge current
  - charge-pump for top-NFETs
  - V_{DS} protection for all NFETs
- Microcontroller:
  - MLX16-FX, application CPU
  - MLX4, communication CPU
  - Programmable digital watch-dog
  - Interrupt controller
  - Common purpose timer
- Memories split per CPU
  - MLX16-FX memories:
    - MLX81346: 64 KB Flash with ECC
    - 20 KB ROM
    - 4 KB RAM
    - 576 Byte EEPROM
  - MLX4 memories:
    - 6 KB ROM
    - 512 Byte RAM
- Fast end-of-line programming via LIN pin (64kB Flash in < 4sec)
- Pin-compatible Predriver family in QFN32
    - MLX81340: 58 KB Flash+ROM
    - MLX81344: 90 KB Flash+ROM
    - MLX81346: 90 KB Flash+ROM
- Periphery
  - Configurable RC-clock 12..32MHz
  - 12x general purpose IO's, digital, analog, 5x high-voltage IO's, 2x UART, SPI, I^2C-slave
  - 2x high-side supply <50mA
  - 5x 16-bit motor PWM timers
  - 2x 16-bit timers
  - 12-bit ADC with < 1.2µs conversion time with 64 channels
  - Differential current sense amplifier with 8-bit programmable overcurrent
  - Temperature sensor, over-temperature detection
  - Over-current detection, over-voltage and under-voltage protection
- Voltage regulators
  - operating motor voltage VSM= 5.5V-60V
  - operating supply voltage VS= 5.5V-32V* (*operating voltage up to 36V limited to 24h over lifetime)
  - Internal voltage regulators, directly powered from VS supply
  - Operation down to 3.5V with reduced analog characteristics, down to 3.0V without losing register content, down to 1.6V with intact RAM memory
  - Low standby current consumption of typ 25µA in sleep mode
  - Wake-up possible via LIN, external pins or internal wake-up timer
- Bus interface
  - LIN 2.x/SAE J2602 and ISO17987-4 compliant LIN slave
- **Automotive AEC-Q100 Qualified**

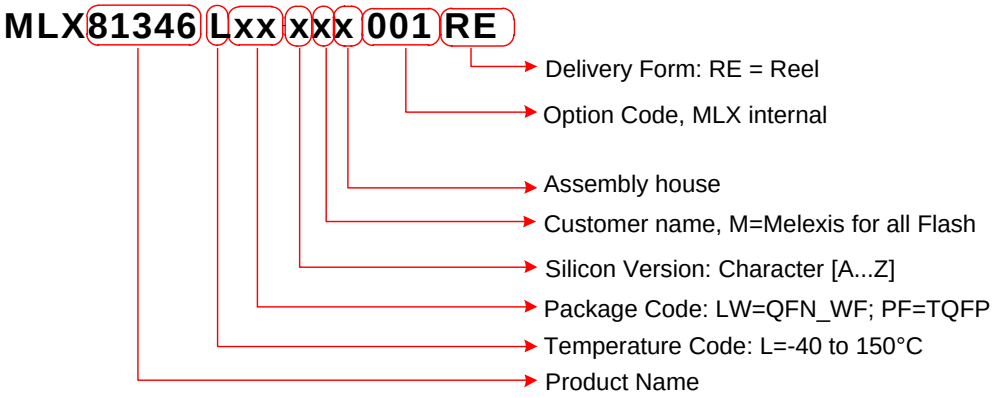
2. Application Examples

- 12V-48V DC/BLDC Engine Cooling Fans, Pumps, Compressors
- 12V-48V DC/BLDC Positioning applications

3. Ordering Information

Order Code	Temp. Range	Package	Delivery	Remark
MLX81346 LLW-BMT-003-RE	-40 - 150 °C	QFN32_WF 5x5	Reel	
MLX81346 LPF-BMA-003-RE	-40 - 150 °C	TQFP48 7x7 eP	Reel	

Table 1 – Ordering Information



4. Family Concept

	MLX81340	MLX81344	MLX81346
MCU Memory	32 KB Flash + 26 KB ROM	64 KB Flash + 26 KB ROM	64 KB Flash + 26 KB ROM
MCU EEPROM	64x 8 Byte	64x 8 Byte	64x 8 Byte
MCU RAM	2.5 KB	4.5 KB	4.5 KB
Pre-Driver	3x Predrivers 60nC gate charge	3x Predrivers 60nC gate charge	3x Predrivers 200nC gate charge
Motor Power range	typ. 10..500W	typ. 10..500W	typ. 10..2000W
Motor Voltage range	5.5V...36V	5.5V...36V	5.5V…60V
IO pins (analog, digital)	9x LV + 3x HV/LV	9x LV + 3x HV/LV	9x LV + 3x HV/LV
Motor current sensing	Low side shunt, differential	Low side shunt, differential	Low side shunt, differential
Sensor interface (3V/5V supply)	analog, pwm, spi, sent, I^2C, uart	analog, pwm, spi, sent, I^2C, uart	analog, pwm, spi, sent, I^2C, uart
Sensorless FOC support	Yes	Yes	Yes
LIN auto-address support (AA)	Yes	No	No
Maximum IC Temperature (with validated mission profile)	T_j = 175°C	Tj = 175°C	Tj = 175°C
Package	QFN32, 5x5 QFN24, 4x4	QFN32, 5x5 QFN24, 4x4	QFN32,5x5 TQFP48, 7x7
Automotive AECQ-100	Yes	Yes	Yes

Table 2 – Famiy Overview

5. Revision history

Version	Date	Description
1.0	01/04/2022	Initial MLX81346 product abstract

Table 3 – Revision history

6. Contents

7. System block diagram and system functions

The system block diagram is shown in Figure 1, where the key system functions of MLX81346 are illustrated, i.e. the capability to drive the phases of a motor over N-FET halfbridges, to read data from sensors and to communicate with the engine control unit (ECU) over a LIN compliant interface.

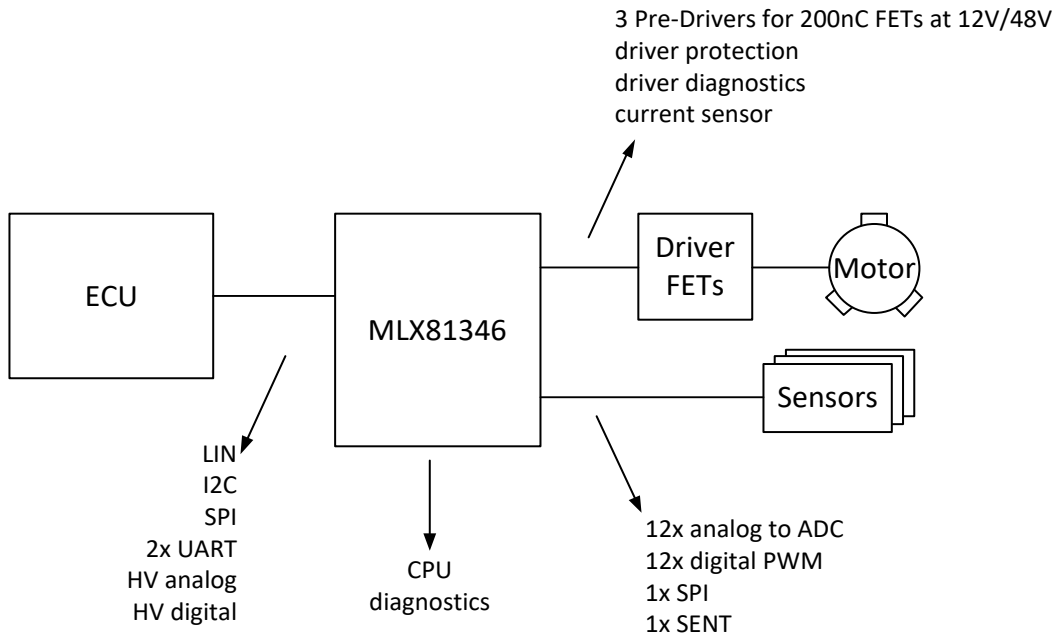


Figure 1 System block diagram

The system functions of MLX81346 are:

- Motor driving:
  - The IC can drive up to 3 half-bridges consisting of 6 N-FETs with max 200nC gate charge to support motors ranging from 10W - 1200W
    - 3-phase BLDC motor
  - The IC can process standard or complex motor drive algorithms
    - Sensor-less FOC (field-oriented control)
    - Sensored FOC (field-oriented control)
- Sensing:
  - The IC senses the motor current over an external shunt
  - The IC can read up to 12 analog outputs of external sensors

  - The IC can read up to 12 digital outputs of external sensors
  - The IC can receive as SPI master the output of an external sensor
  - The IC can receive the SENT output of an external sensor
  - The IC can supply external sensors, limited by maximum supply current <25mA
  - The IC can sense the motor supply and phase voltages

- Communication:
  - The IC supports LIN 2.x, SAE J2602 and ISO17987-4 standards as a slave node
  - The IC supports I^2C Standard-mode, Fast-mode and Fast-mode Plus as a slave node
  - The IC supports the SPI standard
  - The IC can transmit a digital SENT signal
  - The IC can read up to 3 high-voltage analog levels
  - The IC can read up to 3 high-voltage digital signals
  - The IC supports receiving and transmitting a PWM communication signal at the LIN pin
  - The IC supports receiving and transmitting up to 2 UART signals

The diagnostic functions of the IC are covered in the safety manual.

8. Functional safety

The MLX81346 is an ASSP and developed as SEooC [ISO 26262] with assumed technical safety requirements with ASIL-B capability targets. The technical safety concept is described in the MLX81346 Safety manual.

9. IC Block diagram

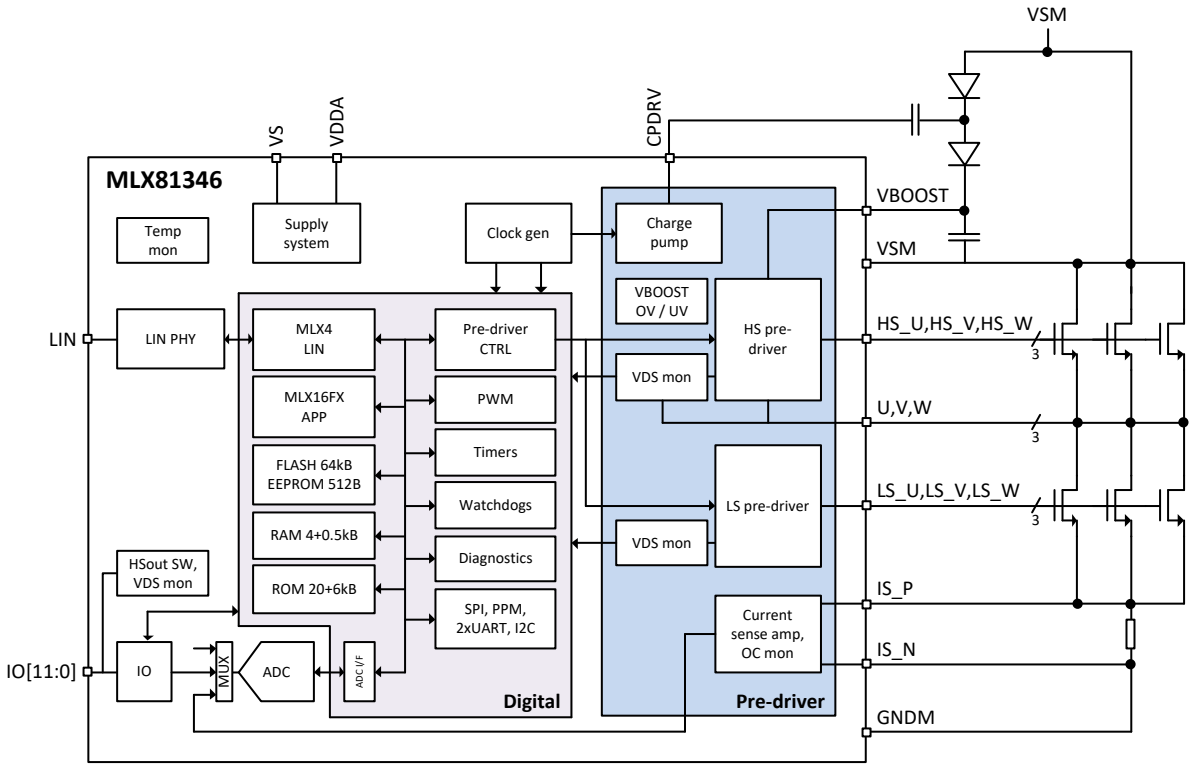
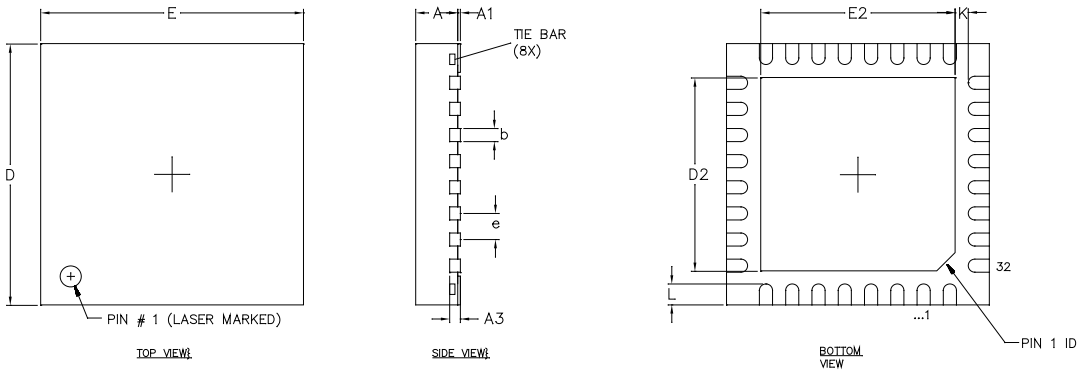


Figure 2 – 81346 IC Block diagram with external power bridge (BLDC)

10. Technical description

10.1. Package data QFN32



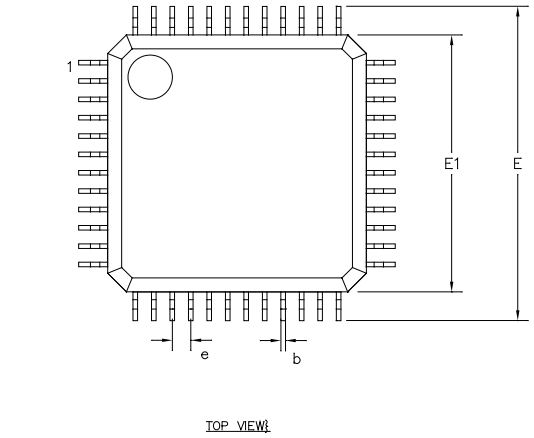
COMMON DIMENSIONS AND TOLERANCES

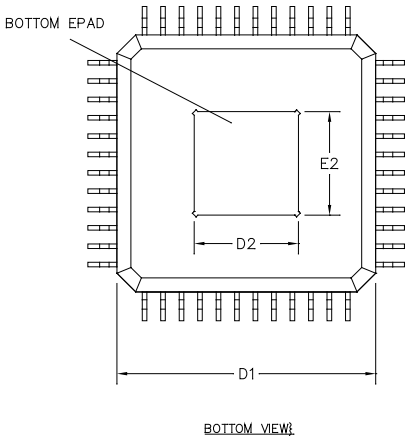
SYMBOL	ALL DIMENSION ARE IN MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
L	0.30	0.40	0.50
K	0.20	---	---
b	0.18	0.25	0.30
e		0.50 BSC	

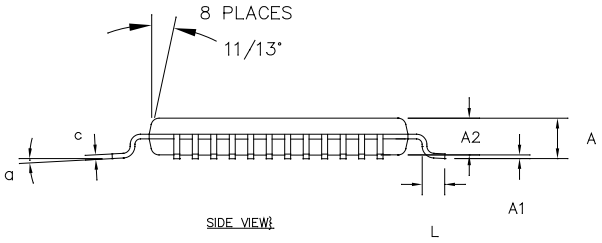
NOTE :
1. EXPOSED TIE BAR SHOULD BE KEPT FREE FROM SOLDER.
2. SIDE WALL IMMERSION TIN PLATING MIN 1um THICK.

Figure 3 – Package data QFN32

10.2. Package Data – TQFP48







Note:
1. DIMENSION D1 AND E1 DO NOT INCLUDE MAX 0.254 mm MOLD PROTRUSION
2. DIMENSION b DOES NOT INCLUDE MAX 0.080 mm DAM BAR PROTRUSION.

COMMON DIMENSIONS AND TOLERANCES

SYMBOL	ALL DIMENSION ARE IN MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
D		9.00 REF	
E		9.00 REF	
D1	6.90	7.00	7.10
E1	6.90	7.00	7.10
D2		5.00 REF	
E2		5.00 REF	
L	0.45	0.60	0.75
b	0.17	0.22	0.27
c	0.09	---	0.20
e		0.50 BSC	
a	0°	---	7°

Figure 4 – Package data TQFP48 7x7 eP

10.3. Package Pin-out

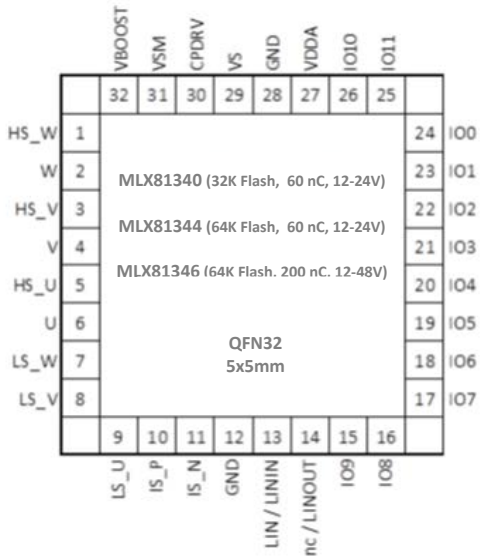


Figure 5 – Pin-out diagram QFN32 (-LLW variant)

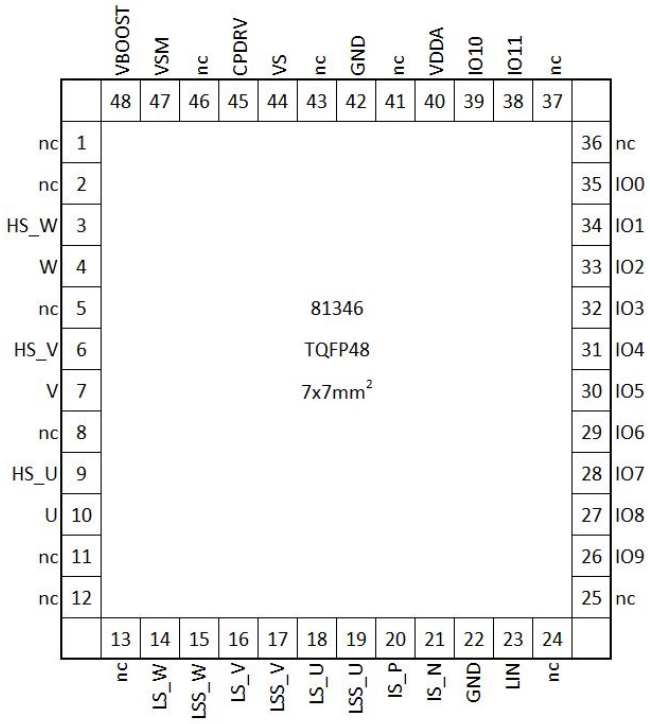


Figure 6 – Pin-out diagram TQFP48 (LPF variant)

10.4. Pin out description

Pin	Pin name	Description	Comment
QFN32, 5x5mm			
1	HS_W	High-Side FET Predriver for W	
2	W	W-phase	
3	HS_V	High-Side FET Predriver for V	
4	V	V-phase	
5	HS_U	High-Side FET Predriver for U	
6	U	U-phase	
7	LS_W	Low-Side FET Predriver for W	
8	LS_V	Low-Side FET Predriver for V	
9	LS_U	Low-Side FET Predriver for U	
10	IS_P	Current sense input (+)	
11	IS_N	Current sense input (-)	
12	GNDM	GND Motor	
13	LIN	LIN interface pin	
14	nc	not connected	
15	IO9	LVIO	
16	IO8	LVIO	
17	IO7	LVIO	1st test interface output TDO
18	IO6	LVIO	1st test interface input TDI
19	IO5	LVIO	
20	IO4	LVIO + HVS (high-voltage supply <50mA)	
21	IO3	LVIO + HVS (high-voltage supply <50mA)	
22	IO2	LVIO + HVIO (high-voltage in/out)	2nd Test interface output TDO
23	IO1	LVIO + HVIO (high-voltage in/out)	2nd Test interface input TDI
24	IO0	LVIO + HVIO (high-voltage in/out)	
25	IO11	LVIO	
26	IO10	LVIO	
27	VDDA	3.3V	3.3V IO supply, option for external sensors ≤

Pin	Pin name	Description	Comment
QFN32, 5x5mm			
			25mA
28	GND	GND IC	
29	VS	Supply IC	For 48V : connect 12V external supply to VS
30	CPDRV	Driver for charge pump	
31	VSM	Supply Motor	
32	VBOOST	Boost voltage to drive High-Side FETs	

Table 4 – Pin-out description for QFN32

#	Pin name	Description	Comment
TQFP48, 7x7mm			
1	NC	Not connected	
2	NC	Not connected	
3	HS_W	High-Side FET Predriver for W	
4	W	W phase	
5	NC	Not connected	
6	HS_V	High-Side FET Predriver for V	
7	V	V phase	
8	NC	Not connected	
9	HS_U	High-Side FET Predriver for U	
10	U	U phase	
11	NC	Not connected	
12	NC	Not connected	
13	NC	Not connected	
14	LS_W	Low-Side FET Predriver for W	
15	LSS_W	GND W phase	
16	LS_V	Low-Side FET Predriver for V	
17	LSS_V	GND V phase	
18	LS_U	Low-Side FET Predriver for U	
19	LSS_U	GND U phase	
20	IS_P	Current sense input (+)	
21	IS_N	Current sense input (-)	
22	GNDM	GND Motor	
23	LIN	LIN interface pin	
24	NC	Not connected	
25	NC	Not connected	
26	IO9	LVIO	
27	IO8	LVIO	
28	IO7	LVIO	1st test interface output TDO
29	IO6	LVIO	1st test interface input TDI
30	IO5	LVIO	

#	Pin name	Description	Comment
TQFP48, 7x7mm			
31	IO4	LVIO + HVS (high-voltage supply <50mA)	
32	IO3	LVIO + HVS (high-voltage supply <50mA)	
33	IO2	LVIO + HVIO (high-voltage in/out)	2nd Test interface output TDO
34	IO1	LVIO + HVIO (high-voltage in/out)	2nd Test interface input TDI
35	IO0	LVIO + HVIO (high-voltage in/out)	
36	NC	Not connected	
37	NC	Not connected	
38	IO11	LVIO	
39	IO10	LVIO	
40	VDDA	3.3V	3.3V IO supply, option for external sensors <25mA
41	NC	Not connected	
42	GND	GND IC	
43	NC	Not connected	
44	VS	Supply IC	For 48V : connect 12V external supply to VS
45	CPDRV	Driver for charge pump	
46	NC	Not connected	
47	VSM	Supply Motor	
48	VBOOST	Boost voltage to drive High-Side FETs	

Table 5 – Pin-out description for TQFP48

10.5. Marking Instruction

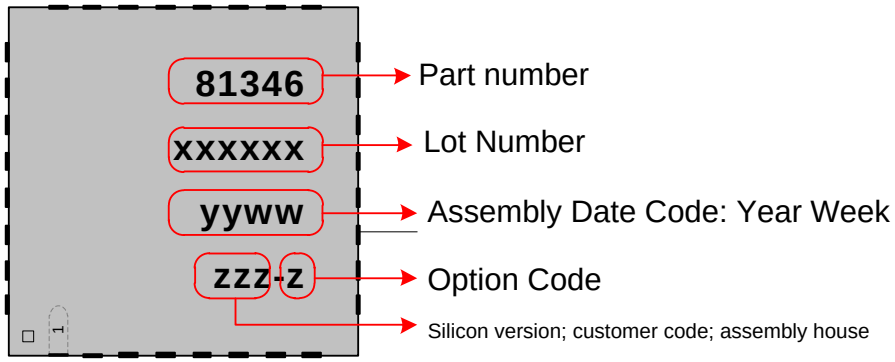


Figure 7 – Marking example on IC package QFN32 5x5

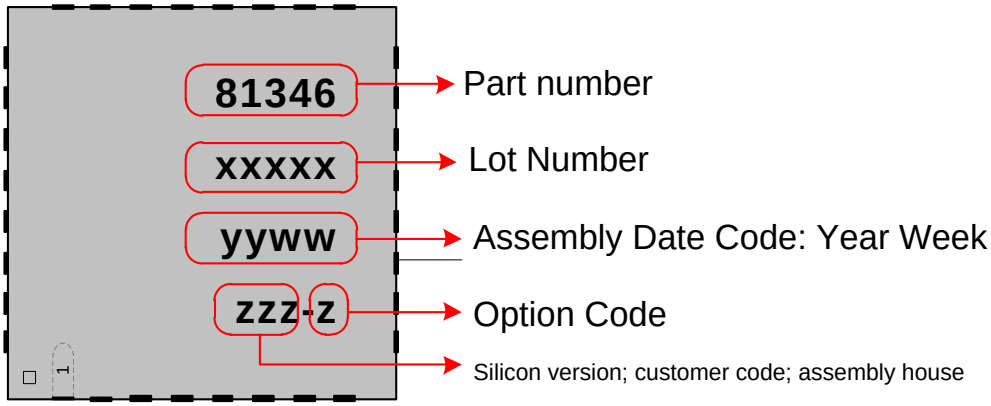


Figure 8 – Marking example on IC package TQFP48

11. Typical application schematic

In the following schematic examples, external components are indicated that may be needed to protect the IC against EMC/ESD pulses. Depending on ECU conditioned power, over-voltage and reverse polarity discretes may be needed. Capcacitor discretes or capacitor values will depend on specific OEM ESD/EMC requirements.

11.1. BLDC Application 12-24V

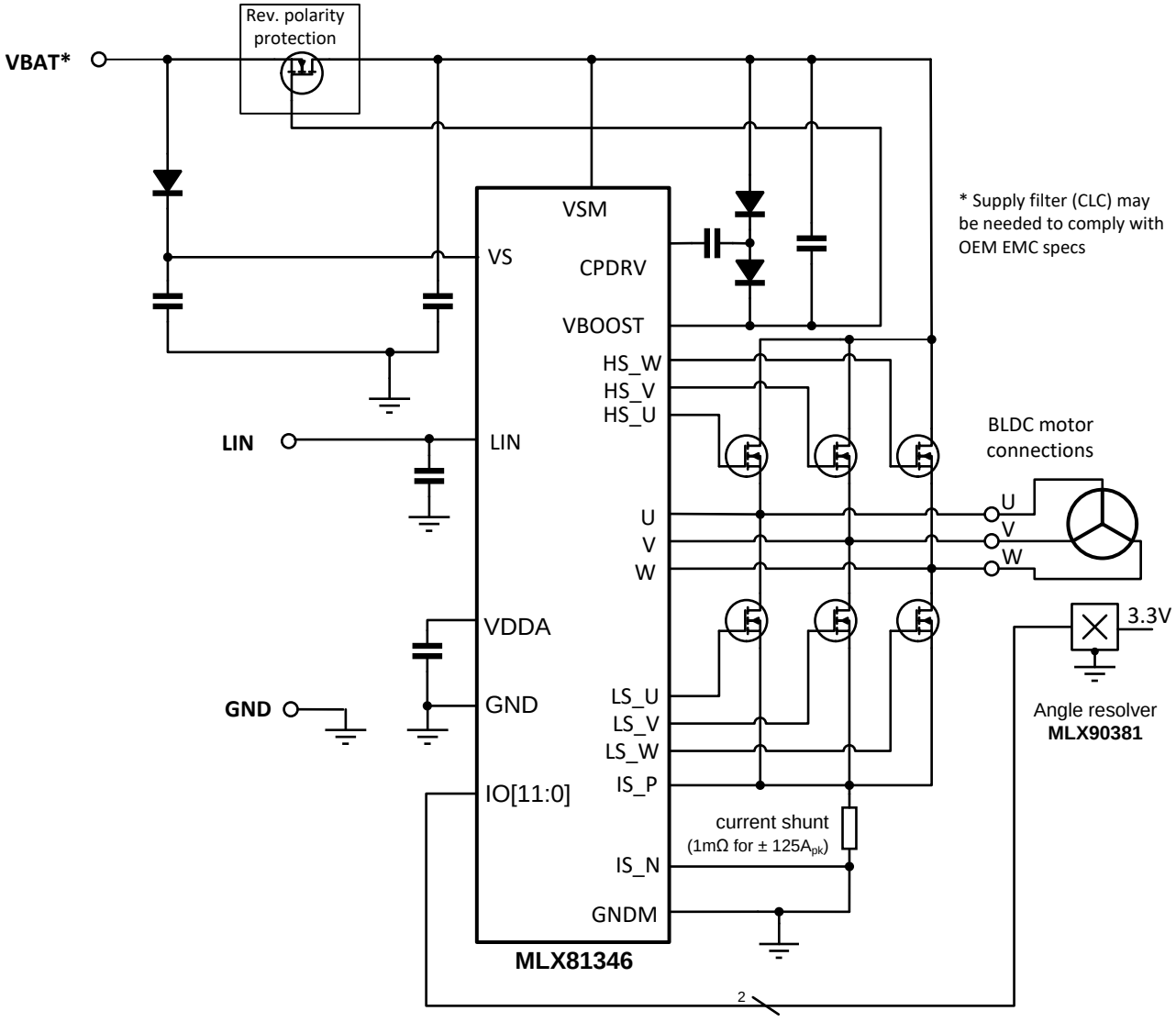


Figure 9 – Typical motor schematic with MLX81346

11.2. BLDC Applications 48V

For 48V automotive applications, 2 changes are needed versus the normal 12V application:

- VS pin is supplied by external 12V regulator to reduce IC heating (linear regulator or DC/DC)
- ECU – Peripheral communication is achieved via capacitive or optical coupling to enable isolation

The concept is shown in below figure:

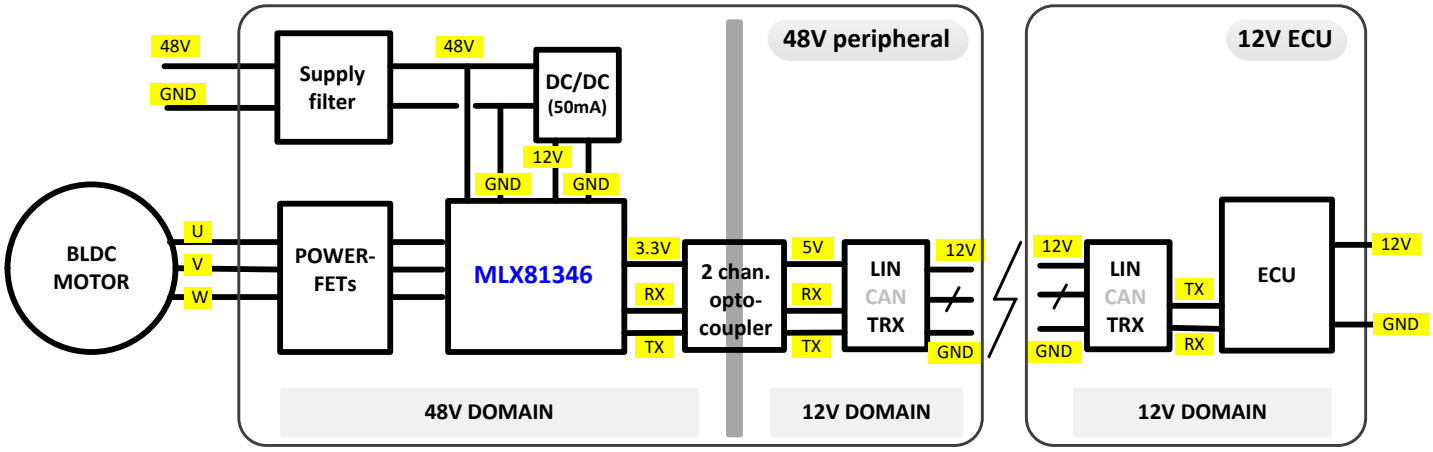


Figure 10 – Principle block diagram for MLX81346 in an isolated 48V application

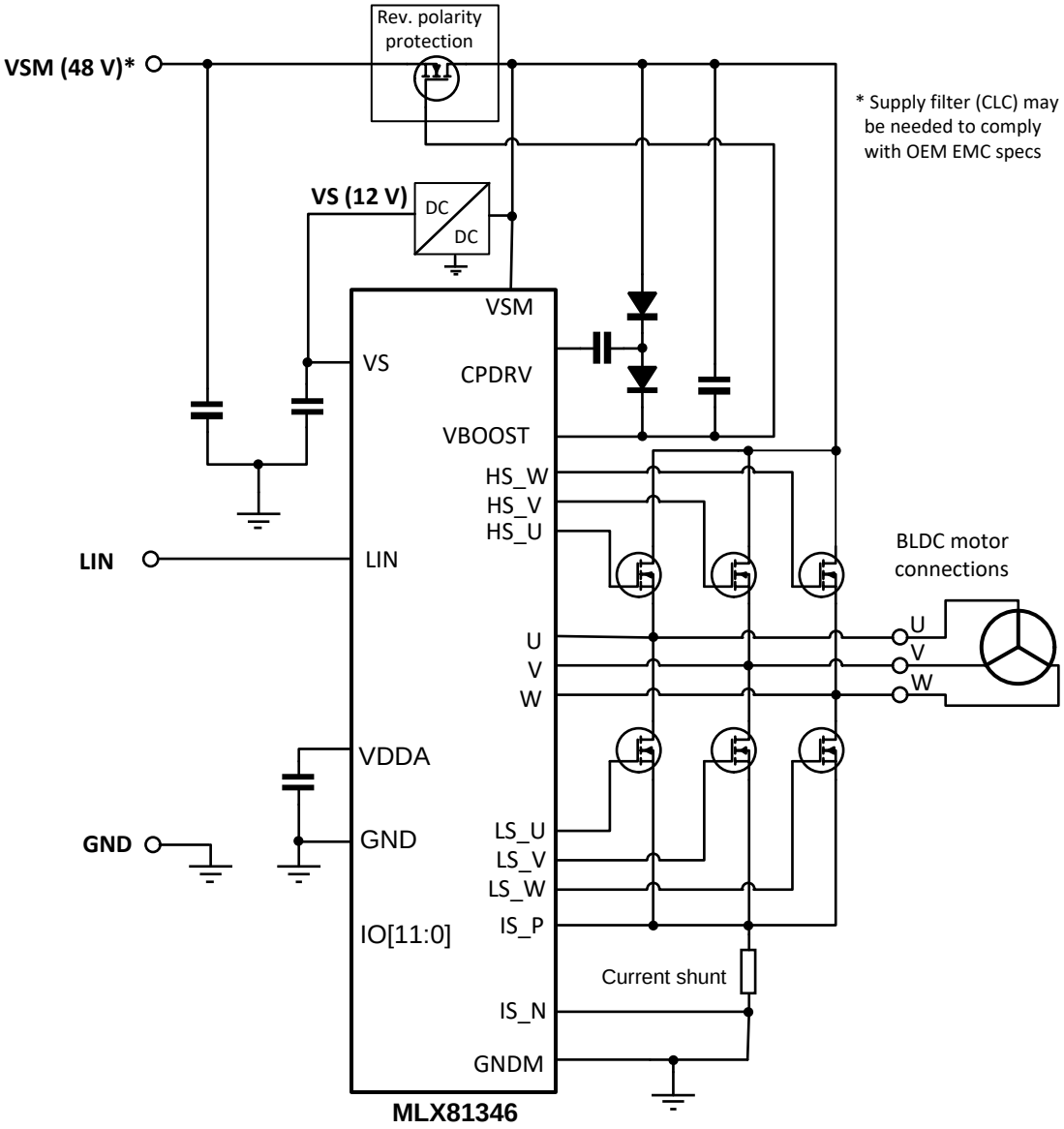


Figure 11 – Principle block diagram for MLX81346 in a 48V application

12. Electrical characteristics

12.1. Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Unit	Condition
Supply voltage IC	VS	-0.5	32 36 [1]	V	
Supply voltage IC	VS	-0.5	45	V	t < 500ms
Supply voltage Motor	VSM	-0.5	60	V	
Supply voltage Motor	VSM	-0.5	70	V	t <500ms [4]
Supply voltage transient	VS.tr1	-100		V	ISO 7637-2 pulse 1 [2]
Supply voltage transient	VS.tr2		75	V	ISO 7637-2 pulse 2 [2]
Supply voltage transient	VS.tr3	-150	100	V	ISO 7637-2 pulses 3a, 3b [2]
Output voltage	VDDA	-0.3	5.5	V	
LIN bus voltage	VLIN	-40	40	V	
LIN bus voltage transient	VLIN.tr1	-30		V	ISO 7637-3 DCC slow - [3]
LIN bus voltage transient	VLIN.tr2		30	V	ISO 7637-3 DCC slow + [3]
LIN bus voltage transient	VLIN.tr3	-150	100	V	ISO 7637-2 pulses 3a, 3b [3]
Analog HV voltage	VAN_HS_U (V,W)	-0.3 -3.0 [4]	VBOOST +0.3	V	HS_U, HS_V, HS_W
Analog HV voltage	VAN_U(V,W)	-0.3 -3.0 [4]	VSM+0.3 VSM+3.0 [4]	V	U, V, W
Analog HV voltage	VAN_LSx	-0.3	10	V	LS_U, LS_V, LS_W
VBOOST voltage	VAN_		70 [5]	V	Switching transients at 60V

[1] 36V operation is limited to maximum 24 hours over life; 28..36V motor driving may require a 100Ω resistor at VBOOST pin for protection reasons in case of PCB switching transients >45V.

[2] ISO 7637 test pulses are applied to VS via a reverse polarity diode and blocking capacitor

[3] ISO 7637 test pulses are applied to LIN via a coupling capacitance of 1nF.

[4] Target for production version – value will be fixed after final qualification

Parameter	Symbol	Min.	Max.	Unit	Condition
	VBOOST				motor drive
IS_P, IS_N voltage	VAN_ISx	-0.3	VDDA+0.3	V	
Analog HV voltage	VAN_HV	-0.3	VS+0.3	V	IO0, IO1, IO2, IO3, IO4 (HV input mode)
Analog LV voltage	VAN_LV	-0.3	VDDA+0.3	V	IO0..IO11
Digital input voltage	VIN_DIG	-0.3	VDDA+0.3	V	IO0..IO11
Digital output voltage	VOUT_DIG	-0.3	VDDA+0.3	V	IO0..IO11
Reverse current into any IO	IREV_IO		1	mA	IO0..IO11
Reverse current into all IO	IREV_IO_TOT		10	mA	IO0..IO11
ESD HBM capability	ESD_HBM	-2	2	kV	All pins
ESD HBM capability	ESD_HBM_LIN	-6	6	kV	Pin LIN. ESD applied on LIN pin versus shorted GND pins
ESD CDM capability	ESD_CDM	-500	500	V	All pins
Junction temperature	TJ	-55	175	ºC	
Thermal resistance QFN32 5x5 [6]	Rth_ja		~32	K/W	in free air
Thermal resistance TQFP48 [6]	Rth_ja		~28	K/W	in free air

Table 6 – Absolute maximum ratings

[5] *80V for <200ms (target for production version 80V for <500ms; will be fixed after final Qualification)*
[6] *Simulated value for low conductance board (JEDEC).*

12.2. Operating range

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply voltage	VS	4	12	32	V	Analog full performance
Supply voltage	VS	3.5		4	V	Analog reduced performance [7]
Supply voltage	VS	32		36	V	Analog reduced performance [8]
Supply voltage	VS	3.0		32 36 [8]	V	Digital functional
Supply voltage	VS	1.6 [4]		32 36 [8]	V	SRAM content valid
Supply voltage	VS	10		32 36 [8]	V	Pre-driver full performance
Supply voltage	VS	5.5		10	V	Pre-driver reduced performance [9]
Motor Supply voltage	VSM	10	12/24 /48	60	V	Operational motor driving
Motor Supply voltage	VSM	5.5		10	V	Operational motor driving reduced performance [9]
Junction temperature	T_J	-40		175	°C	Limited time at T_J=175 °C [10]

Table 7 – Operating range

[7] IC is functional down to 3.5V with reduced analog performance. VDDA short detection may trigger. During IC start-up, VS needs to be >5.5V for a certain time to guarantee a correct reset.

[8] IC is functional up to 36V with reduced analog performance. 36V operation is limited to maximum 24 hours over life; 28..36V motor driving may require a 100Ω resistor at VBOOST pin to protect in case of PCB switching transients >45V.

[9] Pre-driver module is functional with reduced performance (lower gate drive voltage), VBOOST UV may trigger.

[10] Extended temperature range with Tj=175 ºC is only allowed for a limited time, customer's mission profile has to be agreed by Melexis as an obligatory part of the Part Submission Warrant (PSW).

12.3. Electrical specifications

12.3.1. Current consumption

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Normal working current	INOM		10	15	mA	all IO pins are inputs; trimmed to 32 MHz; no external loads; no LIN communication; no ADC conversion
Sleep mode current	ISLEEP		25 100	50 200	µA	VS ≤ 18V, VSM ≤18V, Tj ≤ 150°C VS ≤ 32V, VSM ≤60V, Tj ≤ 150°C
Stop mode current	ISTOP		250	500	µA	
Holding mode current	IHOLD		7		mA	[11]

Table 8 – Electrical specifications: current consumption

12.3.2. Supply system

12.3.2.1. VDDA 3.3V regulator (including 5V option, external C: 0 … 220nF)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
3.3V analog supply voltage	VDDA	3.2	3.3	3.4	V	Bandgap and VDDA regulator trimmed
3.3V external current capability	IDDEXT_ VDDA			25	mA	VS ≥ 4V, external supply for sensors
3.3V under-voltage detection threshold	VTH_UV_ VDDA	2.75	2.85	2.95	V	VDDA ramping down
3.3V under-voltage detection hysteresis	VHYST_ UV_VDDA	0.1	0.175	0.25	V	
Under-voltage debouncing time	TUV_ VDDA	1.0	3.0	10	µs	[11]
3.3V over-voltage detection threshold	VTH_OV_ VDDA	3.85	4.0	4.15	V	VDDA ramping up
3.3V over-voltage detection hysteresis	VHYST_ OV_VDDA	0.1	0.175	0.25	V	
5V analog supply voltage (option)	VDDA5V	4.85	5	5.15	V	Bandgap and VDDA regulator trimmed,

[11] *No production test, guaranteed by design and verified during product verification*

Parameter	Symbol	Min	Typ	Max	Unit	Condition
						SWITCH_VDDA_TO_5V=1
5V external current capability	IDDEXT_ VDDA5V			25	mA	VS ≥ 6V, external supply for sensors
5V under-voltage detection threshold	VTH_UV_ VDDA5V	4.05	4.2	4.35	V	VDDA ramping down, SWITCH_VDDA_TO_5V=1
5V under-voltage detection hysteresis	VHY_UV_ VDDA5V	0.1	0.175	0.25	V	11
5V over-voltage detection threshold	VTH_OV_ VDDA5V	5.6	5.8	6.0	V	VDDA ramping up, SWITCH_VDDA_TO_5V=1
5V over-voltage detection hysteresis	VHY_OV_ VDDA5V	0.1	0.175	0.25	V	
Over-voltage debouncing time	TOV_ VDDA	1.0	3.0	10	µs	11
Short detection threshold	ISH_LH_ VDDA	40.0	65.0	90.0	mA	VS ≥ 4.5V (SWITCH_VDDA_TO_5V=0) VS ≥ 6V (SWITCH_VDDA_TO_5V=1)
Short detection hysteresis	IHYST_SH _VDDA	1.0	1.5	5.0	mA	11

Table 9 – Electrical specifications: VDDA regulator

12.3.2.2. VDDD 1.8V regulator

Parameter	Symbol	Min	Typ	Max	Unit	Condition
1.8V digital supply voltage	VDDD	1.80	1.875	1.95	V	Bandgap and VDDD regulator trimmed
1.8V current capability	IDDINT_ VDDD	15			mA	internal supply only, no external load; for information only

Table 10 – Electrical specifications: VDDD regulator

12.3.2.3. VSM under-voltage and VSM over-voltage detection

Parameter	Symbol	Min	Typ	Max	Unit	Condition
VSM under-voltage detection threshold	VUV_LH_ VS_0	3.5	4	4.5	V	Under-voltage detection on, PRUV_VS=0
VSM under-voltage detection threshold	VUV_LH_ VS_1	4.5	5	5.5	V	Under-voltage detection on, PRUV_VS=1
VSM under-voltage detection threshold	VUV_LH_ VS_2	5.5	6	6.5	V	Under-voltage detection on, PRUV_VS=2

Parameter	Symbol	Min	Typ	Max	Unit	Condition
VSM under-voltage detection threshold	VUV_LH_VS_3	6.5	7	7.5	V	Under-voltage detection on, PRUV_VS=3
VSM under-voltage detection threshold	VUV_LH_VS_4	7.5	8	8.5	V	Under-voltage detection on, PRUV_VS=4
VSM under-voltage detection threshold	VUV_LH_VS_5	8.5	9	9.5	V	Under-voltage detection on, PRUV_VS=5
VSM under-voltage detection hysteresis	VHYST_UV_VS	0.1	0.5	1	V	
VSM under-voltage debouncing time	TUV_VS	1.0	3.0	10	µs	[11]
VSM over-voltage detection threshold	VOV_LH_VS_0	20	22	24	V	Over-voltage detection on, PROV_VS=0
VSM over-voltage detection threshold	VOV_LH_VS_1	22	24	26	V	Over-voltage detection on, PROV_VS=1
VSM over-voltage detection threshold	VOV_LH_VS_2	38	40	42	V	Over-voltage detection on, PROV_VS=2
VSM over-voltage detection threshold	VOV_LH_VS_3	61	64	67	V	Over-voltage detection on, PROV_VS=3
VSM over-voltage detection hysteresis	VHY_OV_VS	1	2	3	V	
VSM over-voltage debouncing time	TOV_VS	1.0	3.0	10	µs	[11]

Table 11 – Electrical specifications: VSM over- and under-voltage detection

12.3.2.4. Wake-up circuit

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Wake-up filter time IO pins	TWU_IO	15		80	µs	SLEEP mode , IO rising & falling edge
Wake-up filter time LIN pin	TWU_LIN	28		145	µs	Time for dominant level after SLEEP mode
Wake-up time internal timer	TWU_INT_0		0			WUI=00 (no wake-up)
Wake-up time internal timer	TWU_INT_1		$\frac{4096}{FRC\_10K}$			WUI=01 (~0.4s)
Wake-up time internal timer	TWU_INT_2		$\frac{8192}{FRC\_10K}$			WUI=10 (~0.8s)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Wake-up time internal timer	TWU_INT_3		$\frac{16384}{FRC\_10K}$			WUI=11 (~1.6s)

Table 12 – Electrical specifications: wake-up circuit

12.3.2.5. Bandgap

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Bandgap voltage	VBG	1.15	1.185	1.22	V	Trimmed
Bandgap voltage temperature coeff.	TC_VBG	0		200	ppm/K	

Table 13 – Electrical specifications: bandgap

12.3.3. Clock generation

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Frequency 1MHz oscillator	FRC_1M	-5%	1	+5%	MHz	
Frequency 32MHz oscillator	FRC_32M	-5%	32	+5%	MHz	MCU clock: MCU_CLK info : 32MHz results in ~25 MIPS
Frequency 10kHz oscillator	FRC_10K	5	10	20	kHz	
Timing accuracy	TIMING_ACC	-1.5		1.5	%	Timing accuracy after sw correction using EEPROM calibration values

Table 14 – Electrical specifications: clock generation

12.3.4. PowerFET Pre-driver

12.3.4.1. Charge Pump and Boost voltage

The charge pump parameters are measured for Cfly = 680nF, Ctank = 3.3µF. Voltages (except hysteresis) are specified relative to VS.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Charge pump clock	FRC_60K	50	60	75	KHz	
VBOOST Charge pump voltage	VBOOST_VS_HI	7.5	9	10	V	VS ≥ 10V, ILOAD ≤ 15mA [12]
VBOOST Charge pump voltage	VBOOST_VS_NOM	5.5	VS -1 [13]	9.5	V	8V < VS < 10V, ILOAD ≤ 15mA [12]
VBOOST Charge pump voltage	VBOOST_VS_LO	3.5	VS -1 [13]	8	V	5.5V < VS < 8V, ILOAD ≤ 5mA [12]
VBOOST Output resistance	RBOOST_OUT		5	20	Ω	
VBOOST under-voltage level	VUV_HL_VBOOST	6.1	6.4	6.7	V	
VBOOST under-voltage hysteresis	VHYST_UV_VBOOST	0.2	0.25	0.35	V	
VBOOST Over-voltage level	VOV_LH_VBOOST	9.5	10.0	10.5	V	
VBOOST Over-voltage hysteresis	VHYST_OV_VBOOST	0.2	0.25	0.3	V	

Table 15 – Electrical specifications: charge pump

12.3.4.2. Predriver stage

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Predriver charge resistance	R_HIGH		8	16	Ω	VSM = 10V… 60V VS ≥ 10V
Predriver discharge resistance	R_LOW		4	8	Ω	VSM = 10V… 60V VS ≥ 10V
Predriver peak charge-current	I_ON		700		mA	5Ω Rgate at FET (200nC)[11]

[12] *Values are valid for BAT54S and similar low forward voltage Schottky diodes with Tj <= 150ºC*
[13] *with BAT54S and estimated 0.4V@ILOAD=10mA at 35°C*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Predriver peak discharge current	I_OFF		1500		mA	5Ω Rgate at FET (200nC) [11]
FET turn-on time	T_ON		200		ns	1V⇨5.5V, 5Ω Rgate at FET (200nC)
FET turn-off time	T_OFF		150		ns	7V⇨1V, discharge diode at FET (200nC)
Interlock delay	T_EILD	0.03		60	µs	Dead-time programmable with 7-bit
FET gate drive voltage		7	9	10	V	VS ≥ 10V [12]
	VPH	5 3	VS-1.5 [13]	9.5 8		8V < VS < 10V [12] 5.5V ≤ VS ≤ 8V [12]

Table 16 – Electrical specifications: predriver stage

12.3.4.3. Current sense amplifier

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input range	V_CSL_IR	-125		125	mV	Current sense range for CSA_HIGHGAIN = 0
Input range	V_CSH_IR	-60		60	mV	Current sense range for CSA_HIGHGAIN = 1
Amplifier low gain	A_CSL	9.5	10	10.5		CSA_HIGHGAIN = 0
Amplifier high gain	A_CSH	19	20	21		CSA_HIGHGAIN = 1
Low-pass filter time		0.25	0.5	1.0	µs	guaranteed by design
Over-current detection level	VTH_OC	10		300	mV	programmable 8-bit DAC (1.56mV/LSB)
Over-current detection accuracy		-10		10	%	FullScale VTH_OC range @VTH_OC 10mV..300mV for Tj<85°C and @VTH_OC 200mV..300mV for Tj=(85..150)°C
Over-current detection accuracy		-10		10	mV	@VTH_OC 10mV...200mV and for Tj=(85..150)°C
Over-current debounce time	TDEB_OC	1		16	µs	programmable 7-bit timer

Table 17 – Electrical specifications: current sense amplifier

12.3.4.4. FET VDS monitor

Parameter	Symbol	Min	Typ	Max	Unit	Condition
VDS over-voltage level	VTH_OV_VDS_0	0.3	0.5	0.7		VDSMON_VTH_SEL = 00
	VTH_OV_VDS_1	0.8	1.0	1.2		VDSMON_VTH_SEL = 01
	VTH_OV_VDS_2	1.3	1.5	1.7		VDSMON_VTH_SEL = 10
	VTH_OV_VDS_3	1.8	2.0	2.2	V	VDSMON_VTH_SEL = 11
VDS over-voltage hysteresis	VHY_OV_VDS	0.05		0.2	V	
VDS over-voltage debounce time	TDEB_OV_VDS	1		16	µs	programmable 7-bit timer

Table 18 – Electrical specifications: FET VDS monitor

12.3.4.5. OSD (off-state-diagnostics)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
OSD Pull up current	I_OSD	150	200	250	µA	
OSD Pull down resistance	R_OSD	25	35	50	kΩ	

Table 19 – Electrical specifications: OSD

12.3.4.6. Active CDI **(Current-Direction-Indicator)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Comparator threshold	VTH_CDI	-7.5	0	7.5	mV	ACTIVE_CDI_CLOCK ≤ 2MHz

Table 20 – Electrical specifications: Active CDI

12.3.4.7. VSM supply sensor

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Voltage range for ADC measurement				36 70	V	Measurement of VSM/26 (VSM_LOWGAIN = 0) Measurement of VSM/52 (VSM_LOWGAIN = 1)
VSM filter cut-off frequency				4	kHz	[11]

Table 21 – Electrical specifications: VSM supply sensor

12.3.5. Over-temperature detection

Parameter	Symbol	Min	Typ	Max	Unit	Condition
OTD threshold	TTH_OT_LH	175	185	195	°C	Temperature ramping up
OTD threshold	TTH_OT_HL		160		°C	Temperature ramping down
OTD hysteresis	THY_OT		25		°C	

Table 22 – Electrical specifications: over-temperature detection

12.3.6. ADC

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Reference voltage	VREF_ADC		1.48		V	Trimmed and calibrated
Resolution			12		bit	ADC cyclic mode for differential input from -VREF_ADC to +VREF_ADC
Sample & Hold time				1	µs	
Conversion time	TCONV		1.125	1.18	µs	ADC_CLK= 16MHz
DNL		-1		1	LSB	[11]
INL		-3		3	LSB	
ADC channel accuracy - LV channels (with 1/2.5		-45		45	mV	0V – 3.3V input, calibrated acc. calibration document [14]

[14] *VS >= 4.5V for HVIO ADC LV channels (IO[4:0]*

Parameter	Symbol	Min	Typ	Max	Unit	Condition
divider)						
ADC channel accuracy - HV channels [15](with 1/26 divider		-0.30		0.30	V	<5V input, calibrated acc. calibration document
ADC channel accuracy - HV channels[15] (with 1/26 divider)		-0.60		0.60	V	<20V input, calibrated acc. calibration document
ADC channel accuracy – U,V,W (with 1/52 divider) and VBOOST (with 1/64 divider)		-1.2		1.2	V	<60V input, calibrated acc. calibration document
ADC channel accuracy - VSMF channel (with 1/26 divider)		-0.20		0.20	V	<5V input, calibrated acc. calibration document
ADC channel accuracy - VSMF channel (with 1/26 divider)		-0.30		0.30	V	<20V input, calibrated acc. calibration document
ADC channel accuracy - VSMF channel (with 1/52 divider)		-0.75		0.75	V	<60V input, calibrated acc. calibration document (w/ and w/o OCD and CSA)
ADC channel accuracy - temperature channel		-10		10	ºC	Calibrated acc. calibration document
ADC channel selection		0		63		

Table 23 – Electrical specifications: ADC

[15] *HV channels are U, V, W, VBOOST, VS, IO0..IO4*

12.3.7. IOs

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input level L⇨H	VTH_LH			2.4	V	IO[11:0]
Input level H⇨L	VTH_HL	1			V	IO[11:0] [16]
Input hysteresis	VHY	0.1			V	IO[11:0]
LV output voltage L	VOL			0.4	V	IO[11:0] (LV-mode) ILOAD = 3mA
LV output voltage H	VOH	VDDA-0.4			V	IO[11:0] (LV-mode) ILOAD = 3mA
LV input range for ADC measurement		0		VDDA	V	IO[11:0] (LV-mode) Measurement of IO[11:0] / 2.5
HV output voltage L	VOL_HV			1.0	V	IO0, IO1, IO2, IO3, IO4 (HV-mode) ILOAD = 5mA
HV output voltage H	VOH_HV	VS-1.0			V	IO0, IO1, IO2, IO3, IO4 (HV-mode) ILOAD = 5mA
HV input range for ADC measurement		0		36	V	IO0, IO1, IO2, IO3, IO4 (HV-mode) Measurement of IOx/26
HS output current				50	mA	IO3, IO4 (HS-mode)
HS output resistance			10	25	Ω	IO3, IO4 (HS-mode)
I2C SDA hold time	TH_SDA	-50	0	50	ns	Referenced to SCL; TRIM_SDAFILT_IO = 00
I2C SDA hold time	TH_SDA	150	260	340	ns	Referenced to SCL; TRIM_SDAFILT_IO = 01
I2C SDA hold time	TH_SDA	200	320	420	ns	Referenced to SCL; TRIM_SDAFILT_IO = 10
I2C SDA hold time	TH_SDA	360	500	640	ns	Referenced to SCL; TRIM_SDAFILT_IO = 11

Table 24 – Electrical specifications: IO

[16] *If IO is connected to an external harness, EMC protection circuitry has to be applied according to paragraph* ***Error! Reference source not found.***

12.3.7.1. VDS monitor IO3 and IO4

Parameter	Symbol	Min	Typ	Max	Unit	Condition
VDS monitor level	VTH _ VDS_IO	70	100	130	mA	VS>=4.5V
VDS monitor hysteresis		5	10	20	mA	
VDS debounce time	TDEB_OV _VDS_IO	0.032		16000	µs	programmable 4-bit timer with 4 bit prescaler

Table 25 – Electrical specifications: VDS monitor IO

12.3.8. LIN

12.3.8.1. LIN transceiver – static [17]

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Transmitter internal capacitance [11]	CLIN		30	40	pF	Response on 14V pulse via 1K
Bus short circuit current	IBUS_LIM	40		200	mA	VLIN = VS = 18V, VTxD = 0V
Pull up resistance bus	RSLAVE	20	35	60	kΩ	VDISTERM = 0
Pull up current bus, sleep mode	ISLAVE_ SLEEP	-50	-20	-5	µA	VLIN = 0V, VSBY = VAUX, VEN =0
Dominant input leakage current including pull up resistor	IBUS_PAS _dom	-1			mA	VLIN =0V, VS =12V, VTxD = VDDD, VDISTERM = 0 VEN = VDDD, VSBY = 0
Recessive input leakage current	IBUS_PAS _rec		0.25	20	µA	VEN = VDDD, VSBY = 0, VTxD = VDDD, VLIN > VS
Bus reverse current loss of battery [18]	IBUS_NO _BAT		0.25	23	µA	VS = 0V, 0V < VLIN ≤18V
Bus current during loss of ground [18]	IBUS_NO _GND	-100		1	µA	VS = VGND = 12V, 0 < VLIN ≤ 18V
Transmitter dominant output voltage [18]	VolBUS	0		0.2×VS	V	Rload = 500Ω
Transmitter recessive output voltage [18]	VohBUS	0.8× VS		1×VS	V	VEN = VDDD, VSBY = 0, VTxD = VDDD or sleep mode
Receiver dominant voltage	VBUSdom			0.4×VS	V	
Receiver recessive voltage	VBUSrec	0.6× VS			V	
Center point of receiver threshold	VBUS_ CNT	0.475 ×VS	0.5× VS	0.525× VS	V	VBUS_cnt = (Vth_dom+ Vth_rec)/2
Receiver hysteresis	VHYS			0.175× VS	V	VHYS = (Vth_rec –Vth_dom)

Table 26 – Electrical specifications: LIN transceiver – static (7 ≤ VS ≤ 18V)

[17] *The parameter in are according to ISO17987-4, SAE J2602-1. For 5.5V < VS < 7V Reduced performance.*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Transmitter internal capacitance [11]	CLIN		30	40	pF	Response on 14V pulse via 1K
Bus short circuit current	IBUS_LIM	40		300	mA	VLIN = VS = 36V, VTxD = 0V
Pull up resistance bus	RSLAVE	20	35	60	kΩ	VDISTERM = 0
Pull up current bus, sleep mode	ISLAVE_ SLEEP	-50	-20	-5	µA	VLIN = 0V, VSBY = VAUX, VEN =0
Dominant input leakage current including pull up resistor	IBUS_PAS _dom	-2			mA	VLIN =0V, VS =24V, VTxD = VDDD, VDISTERM = 0 VEN = VDDD, VSBY = 0
Recessive input leakage current	IBUS_PAS _rec		0.5	20	µA	VEN = VDDD, VSBY = 0, VTxD = VDDD, VLIN > VS
Bus reverse current loss of battery [18]	IBUS_NO _BAT		0.5	23	µA	VS = 0V, 0V < VLIN ≤ 36V
Bus current during loss of ground [18]	IBUS_NO _GND	-200		2	µA	VS = VGND = 12V, 0 < VLIN ≤ 36V
Transmitter dominant output voltage [18]	VolBUS	0		0.2×VS	V	Rload = 500Ω
Transmitter recessive output voltage [18]	VohBUS	0.8×VS		1×VS	V	VEN = VDDD, VSBY = 0, VTxD = VDDD or sleep mode
Receiver dominant voltage	VBUSdom			0.4×VS	V	
Receiver recessive voltage	VBUSrec	0.6×VS			V	
Center point of receiver threshold	VBUS_CN T	0.475× VS	0.5× VS	0.525× VS	V	VBUS_cnt = (Vth_dom+ Vth_rec)/2
Receiver hysteresis	VHYS			0.175× VS	V	VHYS = (Vth_rec –Vth_dom)

Table 27 – Electrical specifications: LIN transceiver – static (18V < VS ≤ 36V)

[18] *In accordance to SAE J2602*

12.3.8.2. LIN transceiver – dynamic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Propagation delay receiver [19] [20]	trx_pdf			6	µs	CRxD =25pF falling edge
Propagation delay receiver [19] [20]	trx_pdr			6	µs	CRxD =25pF rising edge
Propagation delay receiver symmetry	trx_sym	-2		2	µs	Calculate trx_pdf - trx_pdr
Receiver debounce time	trx_deb	0.5		4	µs	LIN rising & falling edge
LIN duty cycle 1 [20] [21]	D1	0.396				20kbps operation, normal mode
LIN duty cycle 2 [20] [21]	D2			0.581		20kbps operation, normal mode
LIN duty cycle 3 [20] [21]	D3	0.417				10.4kbs operation, low speed mode
LIN duty cycle 4 [20] [21]	D4			0.590		10.4kbs operation, low speed mode
tREC(MAX) – tDOM(MIN) [22]	Δt3			15.9	µs	10.4kbs operation, low speed mode
tDOM(MAX) – tREC(MIN) [22]	Δt4			17.28	µs	10.4kbs operation, low speed mode
Slew rate on pin LIN normal mode, trimmed			1.2		V/µs	dV/dt between duty cycle measurement points, VS=12V
Slew rate on pin LIN low speed mode, trimmed			0.6		V/µs	dV/dt between duty cycle measurement points, VS=12V
TxD dominant timeout [23]	ttxd_to		15		ms	Normal mode, vTxD=0V

Table 28 – Electrical specifications: LIN transceiver – dynamic (7 ≤ VS ≤ 18V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Propagation delay receiver [19] [20]	trx_pdf			6	µs	CRxD =25pF falling edge
Propagation delay receiver [19] [20]	trx_pdr			6	µs	CRxD =25pF rising edge
Propagation delay receiver symmetry	trx_sym	-2		2	µs	Calculate trx_pdf - trx_pdr
Receiver debounce time	trx_deb	0.5		4	µs	LIN rising & falling edge
LIN duty cycle 1 [20] [21]	D1	0.330				20kbps operation, normal mode
LIN duty cycle 2 [20] [21]	D2			0.642		20kbps operation, normal mode
LIN duty cycle 3 [20] [21]	D3	0.386				10.4kbs operation, low speed mode
LIN duty cycle 4 [20] [21]	D4			0.591		10.4kbs operation, low speed mode
tREC(MAX) – tDOM(MIN) [22]	Δt3			21.89	µs	10.4kbs operation, low speed mode
tDOM(MAX) – tREC(MIN) [22]	Δt4			17.47	µs	10.4kbs operation, low speed mode
Slew rate on pin LIN normal mode, trimmed			2.4		V/µs	dV/dt between duty cycle measurement points, VS=24V
Slew rate on pin LIN low speed mode, trimmed			1.2		V/µs	dV/dt between duty cycle measurement points, VS=24V
TxD dominant timeout [23]	ttxd_to		15		ms	Normal mode, vTxD=0V

Table 29 – Electrical specifications: LIN transceiver – dynamic (18V < VS ≤ 36V)

[19] *This parameter is tested by applying a square wave signal to the LIN. The minimum slew rate for the LIN rising and falling edges is 50V/µs*
[20] *See Figure 12*
[21] *Standard loads for duty cycle measurements are 1kΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal master termination disabled*
[22] *In accordance to SAE J2602, see Figure 13*
[23] *Parameter in relation to internal signal TxD*

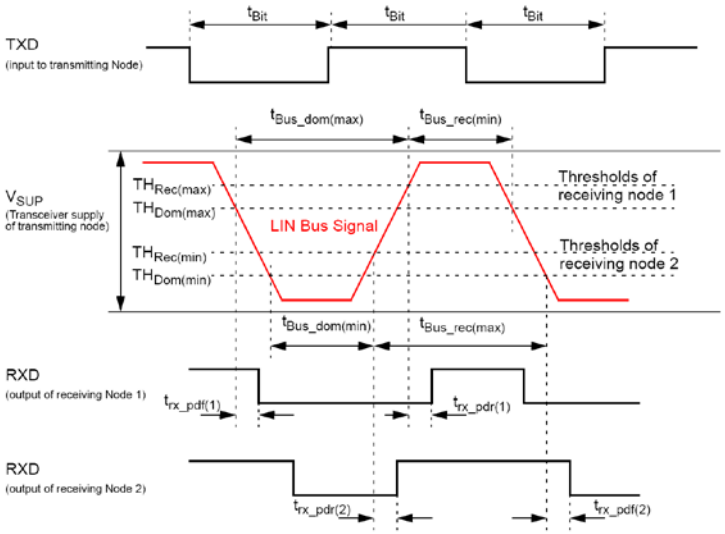


Figure 12 – LIN timing diagram (reference LIN2.1 specification)

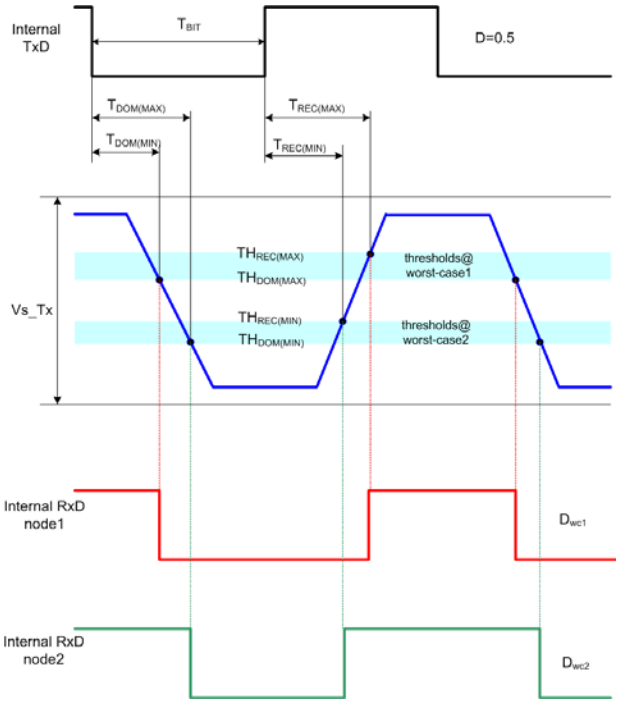


Figure 13 – LIN timing diagram, relation between propagation delay and duty cycle

(Reference SAE J2602 specification)

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The previous versions of this document are repealed.

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