Features

Microcontroller: MLX16-FX RISC CPU

- 16-bit RISC CPU with 20MIPS and Power-Saving-Modes
- Co-processor for fast multiplication and division
- 64 Kbyte Flash, 4 Kbyte RAM, 2 x 256 Byte NVRAM memory with ECC
- In-circuit debug and emulation support

Supported Bus Interfaces:

- LIN interface with integrated LIN transceiver supporting LIN 2.x, SAE J2602; certified LIN protocol software provided by Melexis
- In-Module programming (Flash and NVRAM) via pin LIN using Melexis FastLIN protocol
- PWM interface

Motor Controller

- Patented algorithms for sensor-less 3-phase sine and trapezoidal motor control
- Phase voltage integration filter for BEMF voltage sensing at lowest speeds
- Support of Star and Delta based motor configurations without the need for center star point

Voltage Regulator

- Direct powered from 12V board net with low voltage detection
- Operating voltage VS = 5V to 20.2V
- Internal voltage regulator with possibility to use external regulator transistor
- Very low standby current, < 50µA in sleep mode, wake-up possible via LIN or local sources

Pre-Driver

- Pre-driver for 3 N-FET half bridges with programmable Inter-Lock-Delay for optimal EMC and thermal performance during N-FET switching
- Monitoring of Drain-Source voltages of the N-FETs

Periphery

- Full duplex SPI, Master/Slave, double-buffered, programmable speed, DMA access.
- Full duplex UART
- 4 independent 16-bit timer modules with capture and compare and additional software timer
- 3 programmable 12 bit PWM units with programmable frequencies
- 10 bit ADC converter (2µs conversion time) and DMA access
- On-chip temperature sensor with ±10K accuracy
- System-clock-independent fully integrated watchdog
- 40MHz clock from internal RC oscillator with PLL
- Load dump and brown out interrupt function
- Integrated shunt current amplifier with programmable gain

Applications

The MLX81206/08 IC is designed to control automotive BLDC motors via external FET transistors for 100W..1000W applications like HVAC Blowers, Engine Cooling Fans, Water Pumps, Oil pumps, Compressors and Positioning actuators. IC's are pre-installed with Melexis certified LIN communication stack, and optional support for UDS.

1. Family Overview and Ordering Information

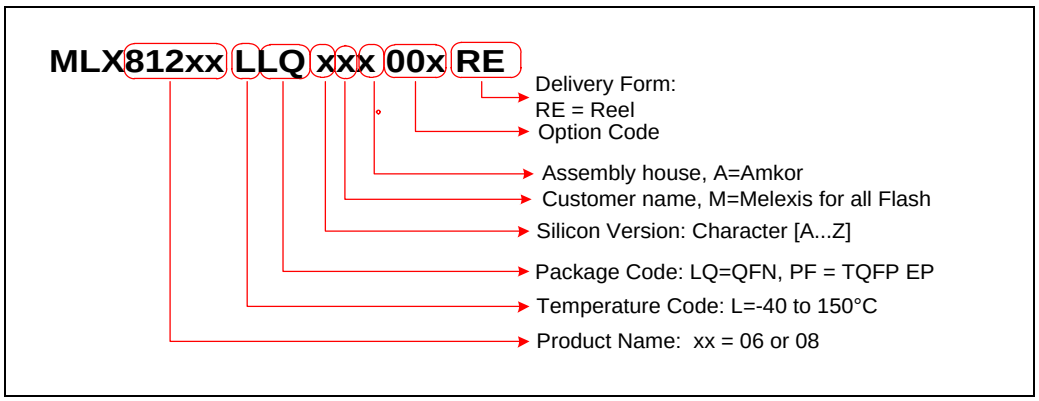
	MLX81205	**MLX81206**	MLX81207	**MLX81208**
Flash Memory [kByte]	32	**64**	32	**64**
ROM Memory [kByte]	6	**6**	6	**6**
RAM [kByte]	4	**4**	4	**4**
NVRAM [Byte] [1]	4x128	**4x128**	4x128	**4x128**
Package	QFN32	**QFN32**	TQFP48	**TQFP48**
Support of active high side reverse polarity protection	No (yes with discretes)	**No** (yes with discretes)	Yes (via CLKO pin)	**Yes** (via CLKO pin)
Current shunt measurement possibility	High side	**High side**	High side	**High side**
SPI	No	**Yes**	Yes	**Yes**
External Crystal option	Yes	**No**	Yes	**No**
UART	Yes	**Yes**	Yes	**Yes**
Number of general purpose IO pins	3	**5**	6	**6**
Support of sensor-based FOC motor control	Yes	**Yes**	Yes	**Yes**
Support of sensorless FOC	Yes	**Yes**	Yes	**Yes**
Bonded pins in package	32	**32**	37	**35**

Table 1 – Family Overview

Order Code	Temperature Range	Package	Delivery	Remark
MLX81206 LLQ-AMA-001-RE	-40 - 150 °C	QFN32 5x5	Reel	
MLX81208 LPF-AMA-001-RE	-40 - 150 °C	TQFP EP 48 7x7	Reel	

Table 2 – Ordering Information

Legend:



[1] *One page of 128 byte is only writable in test mode and reserved for Melexis calibration and test data*

Table of Contents

2. Linked Documentation

MLX16-FX CPU Reference Manual which can be downloaded from http://softdist.melexis.com.

3. Abbreviations and Acronyms

Various abbreviations and acronyms are used throughout this document. Normally bit/register names and symbols of parameters are declared locally in the corresponding chapters with their first occurrence. The table below lists the globally used ones.

Symbol	Equivalent
ADC	Analogue Digital Converter
API	Application Programming Interface, LIN Slave Software for the LIN communication between MLX4 and MLX16-FX CPU's
BLDC	Brush Less Direct Current Motor
Brown Out	Battery under voltage condition, UV_VS
CAN	Controller Area Network, automotive bus standard
CDI	Current Direction Indicator, internal hardware for observing the direction of motor current
AWD	Clock and software independent watchdog. Operates on a separate 10KHz oscillator
CRC	Cyclic Redundancy Checking
Debounce	A filter time, passing signal changes after a specified time being stable, to block noise and disturbances; different styles exist (rising/falling edge only or both edges)
Flash	Large memory containing the User and API software
FSM	Finite state machine, a description of digital behaviour usually used to design sequences of condition action pairs running in a complex loop
ILD	Inter Lock Delay, a blocking mechanism in FET driver circuit preventing a cross current condition on High side and Low side FET of half bridges
IO[5:1]	Arrayed name style for pins IO5, IO4, ….IO1 (IO5 for MLX81208 only)
IOHV	Pin with high voltage feature, for signals with VBAT levels
ISP	In system programming
LIN	Local Interconnect Network, automotive bus standard
Load Dump	Battery over voltage condition, OV_VS
MRB	Master Reset "Bar", the low active main reset for digital part of chip: when active the chip is reset, releasing the processors after going inactive
Mutex	Mutual Exclusion is used to protect shared resources like peripherals and/or RAM locations
NVRAM	Non-volatile RAM, a combined SRAM/RAM block. CPU operates normally on the built-in RAM area (where access is faster) until a permanent storage is required for the time when system is un-powered. By explicitly calling a "save" routine the RAM contents is transferred to SRAM (static RAM)
PLL	phase lock loop, generating the high frequency system clock whose phase is related to the phase of the RCO reference clock 1MHz
POR, PORB	Power On Reset, a partial reset signal indicating a switched on VS voltage
Portsmap	Register bank in digital part, read and/or write able by CPUs

Table 3 – List of abbreviations and acronyms

4. Application Examples [2]

The following sections show typical application examples

4.1. Sensor-less BLDC Motor Control on the LIN bus or via PWM-Interface

The below application example with MLX81206 realizes a sensor-less control of a BLDC motor via three external power N-FET half bridges, with only a few external components. The high side N-FET driver is built with a bootstrap output stage. An external temperature sensor is connected to the 10 bit ADC via pin IO1. The integrated window watchdog is monitoring application integrity. The communication interface can be either LIN or PWM interface. Pins LIN and IOHV can be used as wake-up sources and furthermore pin LIN will be also used to program the Flash memory.

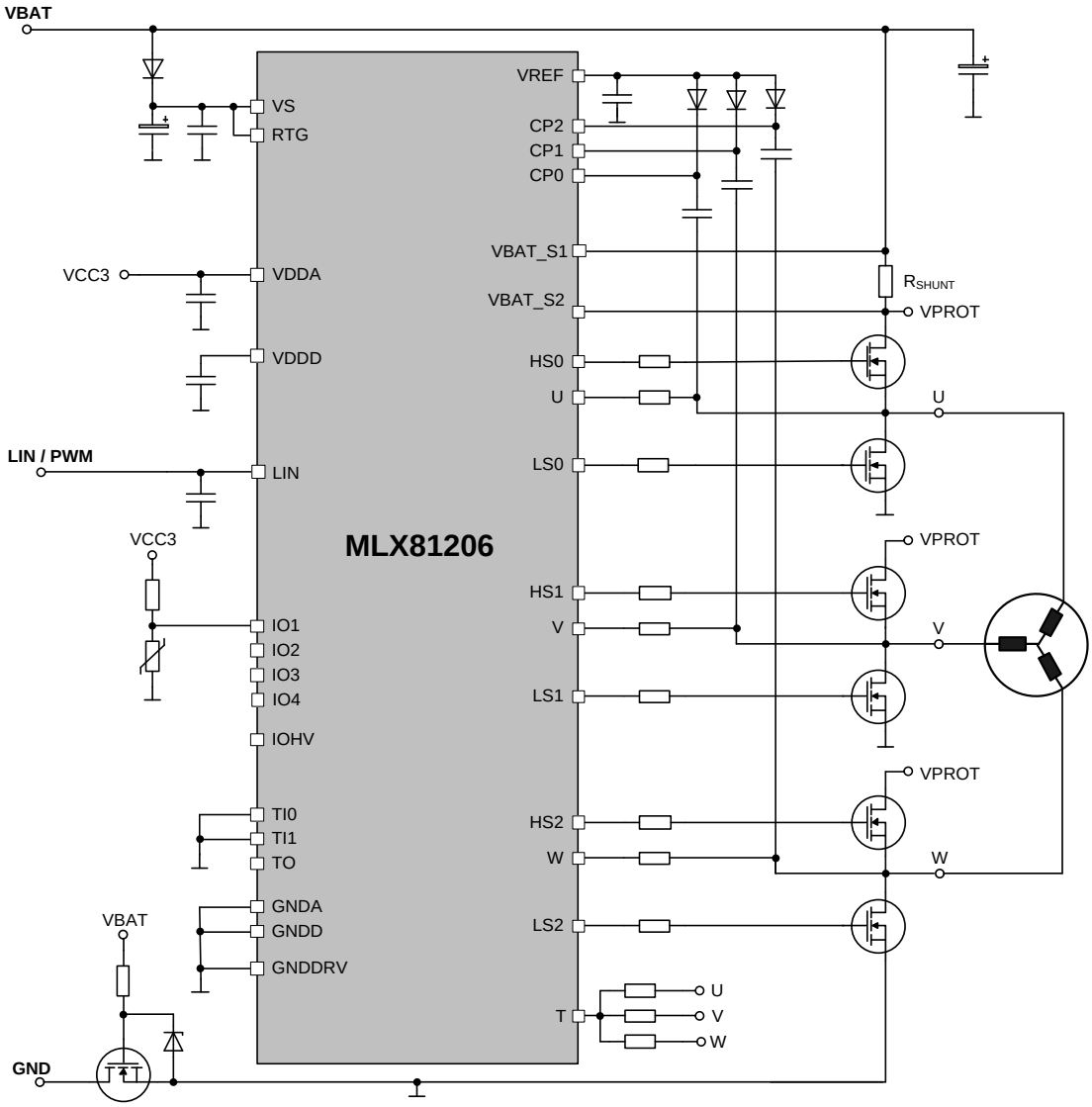


Figure 1. Sensor-less BLDC Motor Control with MLX81206

The motor currents are measured by a shunt resistor in battery path. In case current exceeds the programmed threshold, the bridge can be switched off automatically without software interaction and in addition a software interrupt can be generated. The motor current can also be measured by the 10 bit ADC.

[2] *All application examples are principal schematics only. Please refer to Application Note 'Schematic Design Guide' for application specific details.*

The patented Melexis TruSense technology combines two methods to determine the rotor position:
- The measurement of the induced BEMF voltage at medium and high speeds.
- The measurement of position depending on coil inductance variations at stand-still and low speeds.

As a result TruSense allows operation of the motor in the widest dynamic speed range. The motor can be driven with block, trapezoidal or sine-wave currents. The motor start-up can be made independent of the load conditions according to the application requirements. In this example application the motor star point is not available. It is modelled with external resistors from the motor phases and connected to T input. Alternatively an artificial IC internal reference point can be chosen as shown in the block diagram of the MLX81206/08.

4.2. Sensor-less BLDC Motor Control with LIN Bus or via PWM Interface with reverse polarity protection

In the following sample application the MLX81208 has been selected in order to benefit from the external high side reverse polarity protection option. All other remarks from the previous application example remain valid.

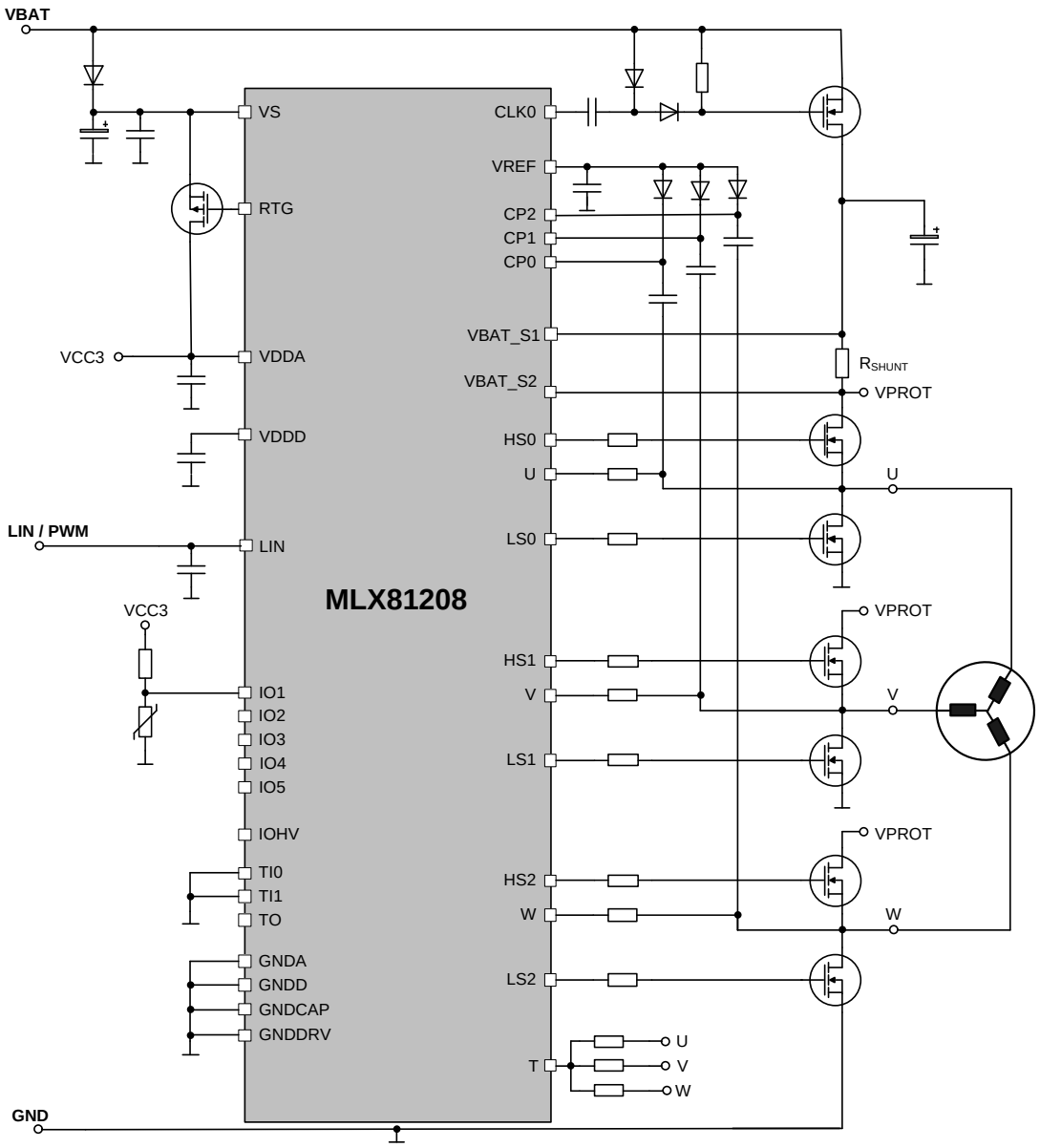


Figure 2. Typical Sensor-less BLDC Motor Control Application Example with MLX81208

4.3. Sensor based BLDC Motor Control

In the sample application below, the MLX81208 drives a BLDC motor with 3 Hall sensors. An external P-FET is used to generate the 3.3V supply with a higher current capability in order to keep the power dissipation outside of the MLX81208 IC.

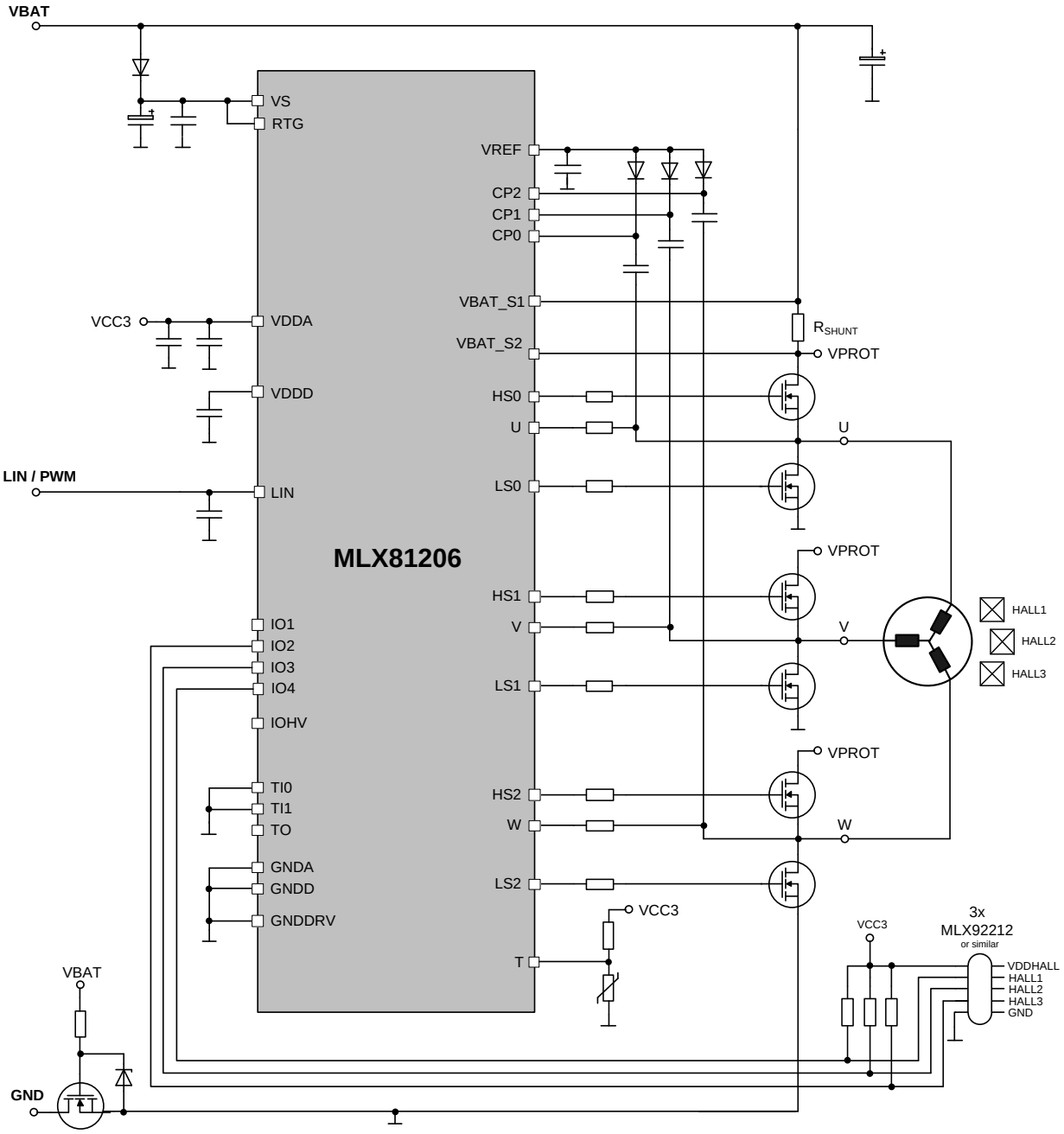
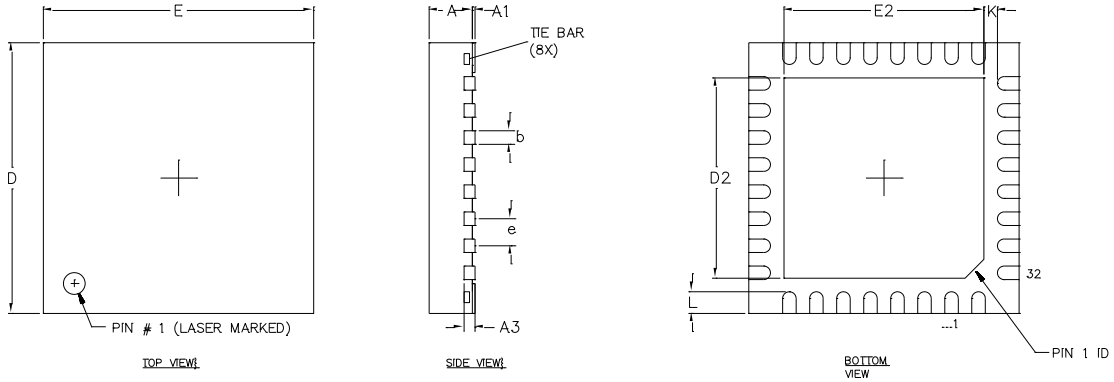


Figure 3. Typical Sensor based BLDC Motor Control Application Example with MLX81208

5. Mechanical Specification

5.1. Package data QFN32 5x5 (32 leads) [3]



COMMON DIMENSIONS AND TOLERANCES

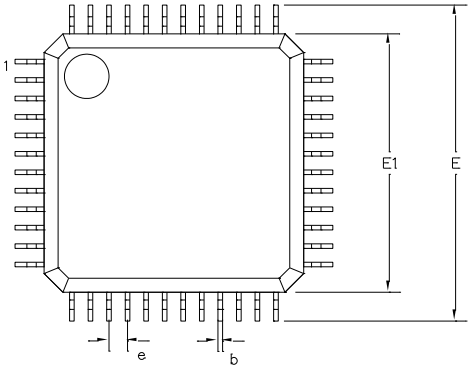
SYMBOL	ALL DIMENSION ARE IN MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
L	0.30	0.40	0.50
K	0.20	---	---
b	0.18	0.25	0.30
e		0.50 BSC	

NOTE :
1. EXPOSED TIE BAR SHOULD BE KEPT FREE FROM SOLDER.
2. SIDE WALL IMMERSION TIN PLATING MIN 1um THICK.

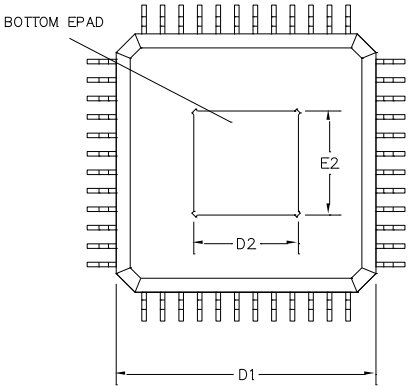
Figure 4. QFN Package Drawing

[3] *Dimensions and tolerances conform to ASME Y14.5M-1994*

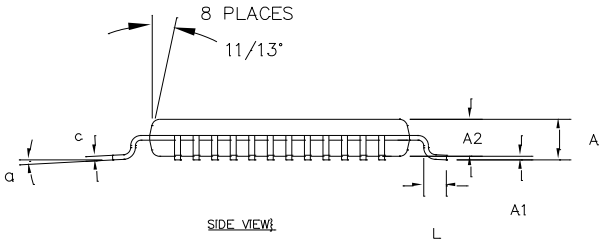
5.2. Package data TQFP package 7x7 (48 leads)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS AND TOLERANCES

SYMBOL	ALL DIMENSION ARE IN MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
D		9.00 REF	
E		9.00 REF	
D1	6.90	7.00	7.10
E1	6.90	7.00	7.10
D2		5.00 REF	
E2		5.00 REF	
L	0.45	0.60	0.75
b	0.17	0.22	0.27
c	0.09	---	0.20
e		0.50 BSC	
a	0°	---	7°

Note:
1. DIMENSION D1 AND E1 DO NOT INCLUDE MAX 0.254 mm MOLD PROTRUSION
2. DIMENSION b DOES NOT INCLUDE MAX 0.080 mm DAM BAR PROTRUSION.

Figure 5. TQFP 7x7 Drawing

5.3. Marking MLX81206/08

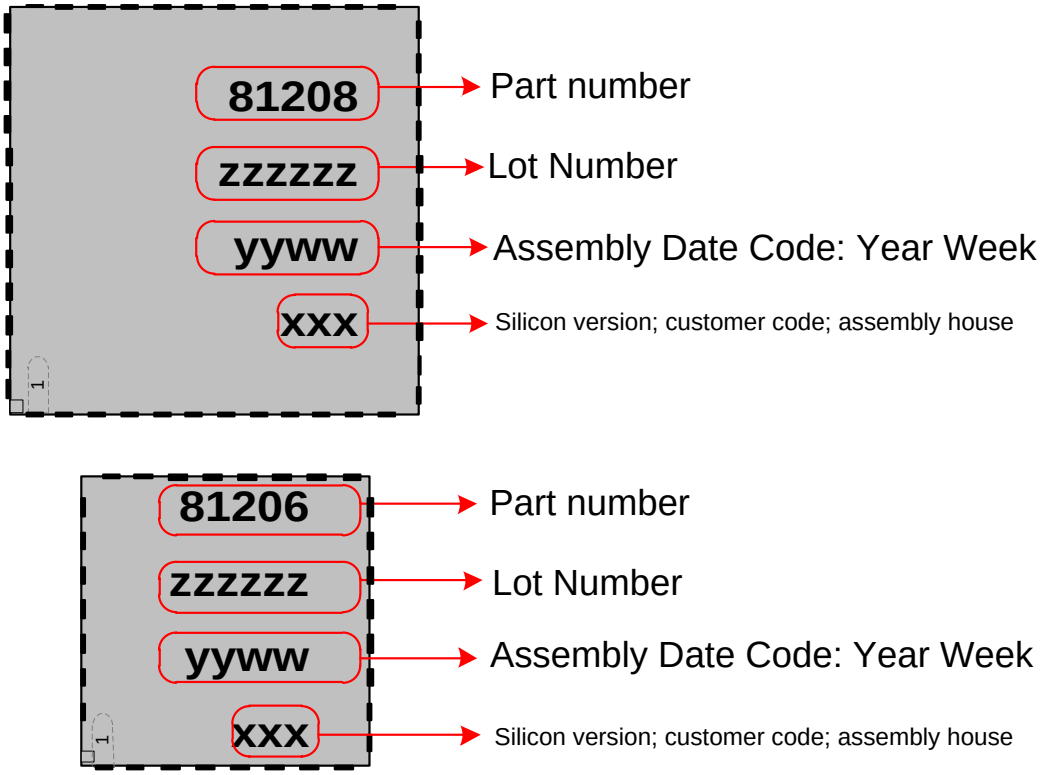


Figure 6. Marking Code

5.4. Pin Description

Name	Type	Function	MLX81206	MLX81208
VS	P	Battery Supply	X	X
RTG	O	3.3V External MOS Gate Control	X	X
VDDA	P	3.3V Supply	X	X
VDDD	P	1.8V Regulator output	X	X
GNDD	GND	Digital ground	X	X
GNDCAP	GND	Digital ground		X
GNDDRV	GND	Driver ground	X	X
GNDA	GND	Analogue ground	X	X
LIN	HVIO	Connection to LIN bus or PWM interface	X	X
IOHV	HVIO	General purpose IO pin	X	X
TI0	I	Test input, debug interface	X	X
TI1	I	Test input, debug interface	X	X
TO	O	Test output, debug interface	X	X
IO1	LVIO	General purpose IO pin (Low voltage 3.3V)	X	X
IO2	LVIO	General purpose IO pin (Low voltage 3.3V)	X	X
IO3	LVIO	General purpose IO pin (Low voltage 3.3V)	X	X
IO4	LVIO	General purpose IO pin (Low voltage 3.3V)	X	X
IO5	LVIO	General purpose IO pin (Low voltage 3.3V)		X

Name	Type	Function	MLX81206	MLX81208
CLKO	HVO	Switchable 250kHz clock output to VREF level		X
T	HVI	Reference input to BEMF sensing blocks	X	X
VREF	P	Clamped 8V or 12V ref. voltage for bootstrapping	X	X
CP2	HVIO	High side bootstrap capacitor driver 2	X	X
HS2	HVIO	N-FET high side gate driver 2	X	X
W	HVI	Phase W input to HS2 buffer and BEMF sensing blocks	X	X
LS2	HVO	N-FET low side gate driver 2	X	X
CP1	HVIO	High side bootstrap capacitor driver 1	X	X
HS1	HVIO	N-FET high side gate driver 1	X	X
V	HVI	Phase V input to HS1 buffer and BEMF sensing blocks	X	X
LS1	HVO	N-FET low side gate driver 1	X	X
CP0	HVIO	High side bootstrap capacitor driver 0	X	X
HS0	HVIO	N-FET high side gate driver 0	X	X
U	HVI	Phase U input to HS0 buffer and BEMF sensing blocks	X	X
LS0	HVO	N-FET low side gate driver 0	X	X
VBAT_S1	HVI	VS high side input for current sensing	X	X
VBAT_S2	HVI	VS low side input for current sensing	X	X

Table 4 – Pin Description MLX81206 / MLX81208

The exposed pad is connected to IC substrate via conductive glue and must be connected to PCB ground.

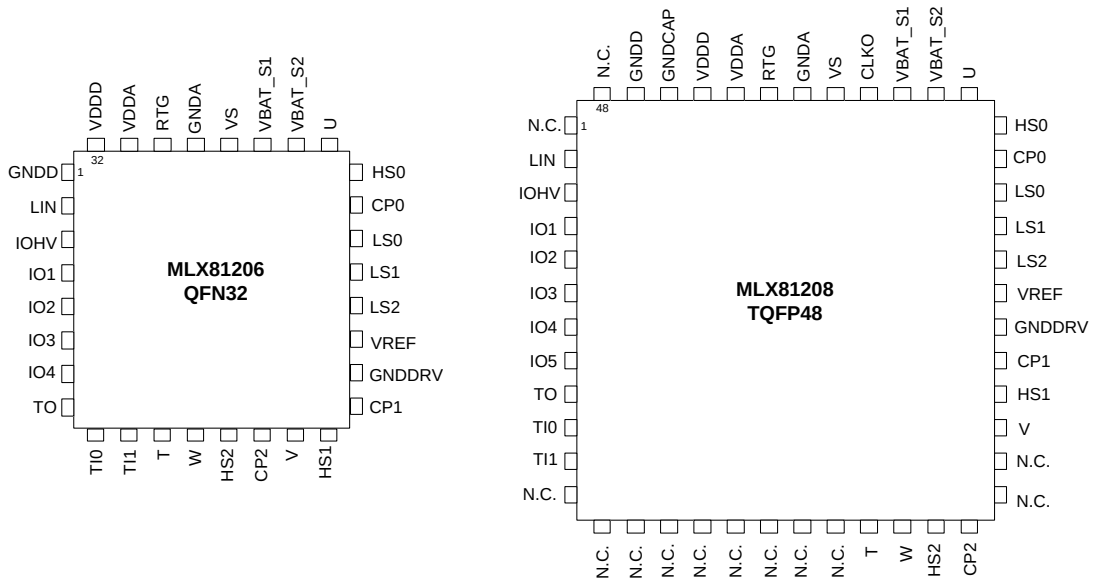


Figure 7. MLX81206/08 Pins

6. Electrical Characteristics

All voltages are referenced to IC ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the MLX81206/08 is only specified within the limits shown in Table 5.

6.1. Operating Conditions

Parameter	Symbol	min	max	Unit
IC supply voltage	VS	5.0	18 (20.2[4])	V
Operating ambient temperature	Tamb	-40	150	°C

Table 5 – Operating Conditions

6.2. Absolute Maximum Ratings

Parameter	Symbol	Condition	min	max	Unit
IC supply voltage on pins VS, VBAT_S1, VBAT_S2	VS	T = 2 min	-0.3	28	V
		T < 500 ms [5]		45	
	VS.tr1	ISO 7637-2 pulse 1 [6] VS=13.5V, TA=(23 ± 5)°C	-100		V
	VS.tr2	ISO 7637-2 pulse 2 [6] VS=13.5V, TA=(23 ± 5)°C		+75	V
	VS.tr3	ISO 7637-2 pulses 3A, 3B [6] VS=13.5V, TA=(23 ± 5)°C	-150	+100	V
	VS.tr5	ISO 7637-2 pulses 5b [6] VS=13.5V, TA=(23 ± 5)°C	+65	+87	V
LIN Bus	VLIN	T<500ms	-27	40	V
	VLIN.tr1	ISO 7637-2 pulse 1 [7] VS=13.5V, TA=(23 ± 5)°C	-100		
	VLIN.tr2	ISO 7637-2 pulse 2 [7] VS=13.5V, TA=(23 ± 5)°C		+75	
	VLIN.tr3	ISO 7637-2 pulses 3A, 3B [8] VS=13.5V, TA=(23 ± 5)°C	-150	+100	
Maximum reverse current into any pin [9]			-10	+10	mA
Maximum sum of reverse currents into all pins [9]				+10	mA
DC voltage on LVIO pins			-0.3	VDDA+0.3	V
DC voltage on pins HV I/O			-0.3	VS+0.3	V
DC voltage on drivers supply pin VREF			-0.3	18	V
DC voltage on pin CLKO			-0.3	VREF+0.3	V
DC voltage on drivers control pins LS<2:0>			-0.5	VREF+0.3	V
DC voltage on drivers pins CP<2:0>		Voltage on pins CP<2:0> must not exceed 45V.	-0.3	V<U,V,W> + 13	V

4 *except Phase integrator*
5 *Only allowed, if FET drivers are disabled, i.e. the high-side driver must not be stressed with V(CP) > 45V.*
6 *ISO 7637 test pulses are applied to VS via a reverse polarity diode and >22µF blocking capacitor*
7 *ISO 7637 test pulses are applied to LIN via a coupling capacitance of 1nF*
8 *ISO 7637 test pulses are applied to LIN via a coupling capacitance of 100pF*
9 *Excluding pins HS0, HS1, HS2, U, V, W, LS0, LS1, LS2*

Parameter	Symbol	Condition	min	max	Unit
DC voltage on drivers pins HS<2:0>		Voltage on pins HS<2:0> must not exceed 45V	-0.5	VS + VREF	V
DC voltage on phases related pins U,V,W [10]	Vph_dc	Voltage on pins U,V,W must not exceed 36V	-0.5	VS+1.5	V
DC voltage on phases related pin T		Voltage on pin T must not exceed 36V	-0.3	VS+1.5	V
Positive dynamic disturbance on pin VBAT_S1 [11]	Vpdd	Spdd > 2 V/µs		4.5	V
ESD capability of pin LIN to GND	ESDLINHB	Human body model, acc. AEC-Q100-002 [17]	-6	+6	kV
ESD capability of pin LIN	ESDLINIEC	acc. IEC 61000-4-2 [12]	-6	+6	kV
ESD capability of pin VS to GND	ESDVSHB	Human body model [17]	-4	+4	kV
ESD capability of any other pins	ESDHB	Human body model [13]	-2	+2	kV
ESD capability ay any pin	ESDCDM	Charge Device Model [14]	-500	+500	V
Maximum latch–up free current at any pin	ILATCH		-250	+250	mA
Junction temperature	Tvj			+155(+175)[15]	°C
Storage temperature	Tstg		-55	+150	°C
R_{thja} QFN32	Rthja	JEDEC 1s2p board		32	K/W
R_{thja} TQFP48eP				28	
R_{thjc} QFN32	Rthjc			10	K/W
R_{thjc} TQFP48eP				5.5	

Table 6 – Absolute Maximum Ratings

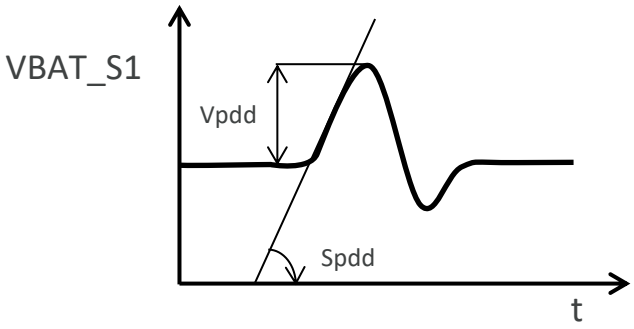


Figure 8. Explanation of Maximum Rating Vpdd

6.3. Electrical Parameter Specification

Following characteristics are valid over the full temperature range of Tj = -40°C to +150°C and a supply range of 5V ≤ VS ≤ 18V unless otherwise noted. With 4.5 V ≤ VS < 5.0 V the controllers are still able to operate and memories keep

10 See also application note for MLX81206/08: "Robustness against negative phase transients during MOSFET switching"
11 *There might be ripple on the VBAT_S1 pin due to parasitic elements in the supply line. Positive voltage peaks with a slew rate larger than Spdd should be limited to Vpdd.(see figure Figure 8) This only applies if the high side current sensor is switched on.*
12 *Equivalent to discharging a 150pF capacitor through a 330Ω resistor conform to IEC Standard 1000-4-2*
13 *Equivalent to discharging a 100pF capacitor through a 1.5kΩ resistor*
14 *Charge Device Model, acc. ANSI/ESDA/JEDEC JS-002*
15 *HTOL with Tj=175°C is ongoing; Tj above 155degC allowed for a limited period of time, customers mission profile has to be agreed with MLX; Some analogue parameter can drift out of specifications, but chip function can be guaranteed*

their contents. However, analogue parameters cannot be fully guaranteed. If several pins are charged with transients above VS and below ground, the sum of all substrate currents of the influenced pins must not exceed 10mA for correct operation of the device.
All voltages refer to IC ground, which is achieved by an external connection of all ground pins on the PCB. Ground pins are not connected inside the MLX81206/08 in order to meet EMC requirements and minimize noise coupling.

6.3.1. Global Parameters and Clocks

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Global Parameters						
Normal operation current	I_NOM	FPLL=40MHz, no external DC-load		25	30	mA
Sleep mode current	I_SLEEP	VS = 13V, T ≤ 35°C			30	µA
		VS = 13V			50	µA
		VS = 18V			100	µA
Startup time of system after Power-On	Tstartup	Internal 3.3V supply: Cap.@VDDA=100nF Cap.@VDDD=100nF Time between VS exceeding POR level and master reset is released (MRB). Not tested in production; for information only.			1	ms
Startup time of system after WAKE UP from Sleep mode	Tstartup_sleep	Internal 3.3V supply: Cap.@VDDA=100nF Cap.@VDDD=100nF Time between WAKE UP command and master reset is released (MRB). Not tested in production; for information only.			0.75	ms
1MHz RC Oscillator						
Frequency of trimmed system RC oscillator	F_RC1M	After calibration.	0.95	1.0	1.05	MHz
10kHz RC Oscillator for Watchdog						
Frequency	F_10K		5	10	20	kHz
Temperature dependency	F_10K_DT	Referred to F_10K	-10		10	%
PLL system clock						
PLL output frequency	F_PLL	according PLL_DIV, PLL input frequency = 250kHz	12		40	MHz
PLL frequency accuracy	Delta_fpll	Chip trimmed according Melexis trimming procedure.	-5		5	%
Settling time of PLL	T_SETPLL				250	µs

Table 7 – Global Parameters and Clocks

6.3.2. Supply System, Temperature Sensor and CLKO Pin

Parameter	Symbol	Test Conditions	min	typ	max	Unit
VDDA Parameters Internal supply: max. ESR of capacitors < 200mΩ total capacitance at pin VDDA: w/o external PMOS: Cext_vdda = 100nF … 220nF; w/ external PMOS: Cext_vdda ≥ 6.8µF … 10 µF						
3.3V supply voltage range	VDDA	After trimming	3.135	3.3	3.465	V

Parameter	Symbol	Test Conditions	min	typ	max	Unit
External output current capability		For information only[16]			10	mA
Undervoltage reset on	VUVR_HL_VDDA		2.7	2.85	3.0	V
Undervoltage reset off	VUVR_LH_VDDA		2.85	3	3.15	V
Hysteresis for undervoltage reset	VHYST_UVR_VDDA		0.1			V
Debouncing for UVR	TUVR_VDDA		1	3	10	µs
VDDD Parameters (MLX81206/08: Cext_vddd = 47nF … 220nF)						
1.8V supply voltage range	VDDD		1.77	1.85	1.98	V
External output current capability					0	mA
Undervoltage reset on	Vuvr_hl_VDDD		1.525	1.6	1.675	V
Undervoltage reset off	Vuvr_lh_VDDD		1.6	1.675	1.75	V
Hysteresis for undervoltage reset	Vhyst_uvr_VDDD		0.05		0.225	V
Debouncing for UVR	tuvr_VDDD		1	3	10	µs
Power-On Reset Parameters (VS based, for information only)						
POR off	Vpor_lh		2.9	3.6	4.1	V
POR on	Vpor_hl		2.4	3.15	3.6	V
Hysteresis for POR	Vhyst_por		150		1300	mV
VS – programmable under voltage interrupt parameters (on pins VS and VBAT_S1)						
Programmable range for under voltage level	Vuv_range	PRUV[1:0]: 00	5.0	5.5	6.0	V
		PRUV[1:0]: 01	6.5	7.0	7.5	
		PRUV[1:0]: 10	7.5	8.0	8.5	
		PRUV[1:0]: 11	8.5	9.0	9.5	
		PRUV_VBAT[1:0]: 00	5.0	5.5	6.0	V
		PRUV_VBAT[1:0]: 01	6.5	7.0	7.5	
		PRUV_VBAT[1:0]: 10	7.5	8.0	8.5	
		PRUV_VBAT[1:0]: 11	8.5	9.0	9.5	
Hysteresis for under voltage	Vhyst_uv_VS		0.1		1.0	V
Debouncing for under voltage	tuv_VS		10	30	130	µs
VS – Over voltage (Load dump) interrupt related parameters						
Level for load dump interrupt	Vldh		29	31	33	V
Hysteresis for load dump interrupt	Vhyst_ld		1	2	3	V
Debouncing for load dump interrupt	TLD		50		100	µs
VREF Parameters						
Reference voltage	VREF	VS=18V, VREF_SEL=0, ILOAD = 50mA	7	8.5	9.5	V
Reference voltage	VREF	VS=18V, VREF_SEL=1, ILOAD = 50mA	11	12	13	V
Min. reference voltage	VREFMIN	VS=6V, ILOAD = 50mA	3.5	4.6	5.5	V
Output current to trigger	VREF_ERR	T_debounce > 100 µs	55	70	120	mA

[16] *For higher external current the external p-mos solution needs to be used. Customer also needs to take care for the max. allowed Tj.*

Parameter	Symbol	Test Conditions	min	typ	max	Unit
VREF_ERR [17]						
Over Temperature Sensor for IR						
Over Temperature IR: OVT	Tot_on	tested by special test mode only	160	170	180	°C
	Tot_off		130	140	150	°C
	Tot_hyst	guaranteed by design	10			K
Temperature Sensor for ADC Measurement						
Temperature range	Trange	For information only.	-40		+150	°C
Accuracy	Tacc	For information only.	-10		+10	°C
CLKO Pin (only MLX81208)						
Output voltage swing	VOUT_H	ILOAD = 1mA, VS=13V	VREF-0.5V		VREF	V
	VOUT_L	ILOAD=1mA, VS=13V	0.0		0.5	V
Digital input threshold level L => H	VinCLKO		1.2		2.4	V
Digital input threshold level H => L	vinlCLKO		1.2		2.4	V

Table 8 – Supply System, Temperature Sensor and CLKO Pin

6.3.3. 10 bit ADC

Parameter	Symbol	Test Conditions	min	typ	max	Unit
10 bit ADC						
Reference voltage high	VREF2	SREF[0] = 1	2.46	2.5	2.54	V
Differential nonlinearity [18]	DNL	ADC-Clock ≤ 5.2 MHz	-1		+1	LSB
Integral nonlinearity [21]	INL	ADC-Clock ≤ 5.2 MHz	-3		+3	LSB
Conversion Time	TCONV	ADC-Clock = 5.2 MHz		2		µs
Resistor divider mismatch	ATTERR	Channels w/ internal divider			2	%

Table 9 – 10 bit ADC electrical parameter

6.3.4. High Side Current Sensor on Pins VBAT_S1 and VBAT_S2

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Over Current Comparator						
Input offset [19]	VOFF				5	mV
Gain Amplifier						
Input voltage range [20]	VIN	VBAT_S1-VBAT_S2, Gain=10	0		200	mV

17 *This parameter specifies the limits for the error generation VREF_ERR. In order to avoid destruction in case of overload, the VREF supply has also a built in current limiting function, which clamps the VREF current at max of 120mA*
18 *Not tested on production test, guaranteed by design. This parameter is for information only evaluated during characterization to hold the specified range*
19 *Not tested during production test, guaranteed by design. This parameter is for information only and was measured during characterization in the specified range*
20 *Calculated value based on 2.5V DAC reference voltage and offset and gain values*

Parameter	Symbol	Test Conditions	min	typ	max	Unit
		VBAT_S1-VBAT_S2, Gain=25	0		75	
		VBAT_S1-VBAT_S2, Gain=40	0		40	
Amplifier output when input is zero [21]	VOFF	OC_CFG[2:1]=00 (Gain = 10)	0	65	300	mV
		OC_CFG[2:1]=01 (Gain = 25)	0	180	500	
		OC_CFG[2:1]=10 (Gain = 40)	0	280	750	
Amplifier offset calibration error measured at amplifier output	CALERR	OC_CFG[2:1]=00 (Gain=10), VBAT_S1 = VS, VBAT_S2 connected via 27Ω to VBAT_S1: Amplifier_OUT (OFFSCAL = 0) - Amplifier_OUT (OFFSCAL = 1)	-20		20	mV
		OC_CFG[2:1]=01 (Gain=25), VBAT_S1 = VS, VBAT_S2 connected via 27Ω to VBAT_S1: Amplifier_OUT (OFFSCAL = 0) - Amplifier_OUT (OFFSCAL = 1)	-45		45	mV
		OC_CFG[2:1]=10 (Gain=40), VBAT_S1 = VS, VBAT_S2 connected via 27Ω to VBAT_S1: Amplifier_OUT (OFFSCAL = 0) - Amplifier_OUT (OFFSCAL = 1)	-80		80	mV
Gain	GAIN_HS	OC_CFG[2:1]=00 (Gain = 10)	9.7	10.0	10.4	
		OC_CFG[2:1]=01 (Gain = 25)	24.0	25.0	26.0	
		OC_CFG[2:1]=10 (Gain = 40)	38.5	40.0	41.5	
Bias current [22]	IBIAS	Pin VBAT_S1		170		µA
Output Settling Time [23]	TSETT	Max. output jump to within 99% final value measured afterADC	0	2	2.5	µs
8 bit DAC						
Reference voltage high	VRH		2.45	2.5	2.55	V
Differential nonlinearity [24]	DNL		-1		+1	LSB

21 *The actual amplifier offset can be measured with the ADC by using bit OFFSCAL. When a high accuracy is needed the offset should be measured with the ADC when current through the shunt is zero, i.e. at instances of time during the PWM period, when the motor current is forced through the LS NFETs*

22 *Because the amplifier is supplied via pin VBAT_S1, a low ohmic connection from shunt to MLX812xx is needed in the application*

23 *Not tested on production test, guaranteed by design. This parameter is for information only evaluated during characterization to hold the specified range.*

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Settling time	Tsettling_DAC8	Information parameter, not tested in production		10		µs
Current Sources						
Pull-down current VBAT_S1	Ipd_sw	OC_CS[2]=1	6	10	15	µA
Pull-down current VBAT_S2	Ipd_sw	OC_CS[3]=1	6	10	15	µA

Table 10 – High side over current electrical parameters

6.3.5. Phase Integration Filter and BEMF Comparators

Parameter	Symbol	Test Conditions	min	typ	max	Unit
BEMF Comparator						
Input voltage range	VINCOM	Pins U,V,W	0		VS	V
		Pin T	$\frac{VS}{3}$	$\frac{VS}{2}$	$\frac{2}{3}VS$	V
Comparator hysteresis	VTHR	BEMF_COMP[6]=1		50	200	mV
		BEMF_COMP[6]=0		15	100	mV
Phase Integrator, multiplexed on U,V,W and T (or VBAT_S1 / 2)						
Common mode input range [25]	VCOM	Pins U,V,W	0		VS	V
		Pin T	$\frac{VS}{3}$	$\frac{VS}{2}$	$\frac{2}{3}VS$	V
Extended common mode input range [25]	VCOM_ext	Pins U,V,W, T	0.15		VS-0.15	V
Integrator output at zero input	Vphref1	U,V,W = T, TINT = 5µs	1.0	1.25	1.5	V
Calibration Error	CAL_ERR	Measured as difference between integrator output with max. diff. input voltage, bit PH_CAL=1, TINT=5 µs and Vphref1	-20	0	20	mV
Diff. input voltage U,V,W -T	VIN		$\frac{-VS}{2}$		$\frac{VS}{2}$	V
Output voltage gain	VGAIN	Tint=8 µs, VIN=3V, INTEGRATION mode, after trimming	2.16	2.4	2.64	V
		Tint=8 µs, VIN=-3V, INTEGRATION mode, after trimming	0	0.1	0.35	V

Table 11 – Phase Integration Filter and BEMF comparator electrical parameter

6.3.6. Pins IO[5:1] (IO[4:1] for MLX81206) and IOHV

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Pins IO[5:1]						
Leakage current in IO[5:1]	Ileakio[5:1]	Res. divider in ADC disabled	-1		1	µA

[24] *Not tested during production test, guaranteed by design. This parameter is for information only and was measured during characterization to hold the specified range*

[25] *The accuracy of the phase integrator measurement specified in this table cannot be guaranteed, if the input voltages are not within either VCOM or VCOM_ext input ranges*

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Digital input threshold level L => H	Vinhio[5:1]		1.8		2.4	V
Digital input threshold level H => L	vinlio[5:1]		0.8		1.6	V
Digital output voltage high	IOOUTH[5:1]	Iload = 2mA	2.9		3.4	V
Digital output voltage low	IOOUTL[5:1]	Iload = 2mA	0		0.4	V
PIN IOHV – Wake-Up Comparator (VAUX supplied)						
WU input threshold level L => H	WU_LH		1.2		2.4	V
WU input threshold level H => L	WU_LH		1.2		2.4	V
PIN IOHV – Analogue Comparator (VS supplied)						
Leakage current	Ileakiohv	Res. divider in ADC disabled	-5		5	µA
Comperator ratiometric threshold level, high threshold	IOHV_HL IOHV_LH	H => L L => H	0.4 0.5	0.45 0.55	0.5 0.6	VS
PIN IOHV – Pull-up, Pull-down Current Source						
Pull-up current	IOHV_PU		-15	-30	-45	µA
Pull-down current	IOHV_PD		15	30	45	µA
PIN IOHV – Open Drain Output						
Outpt Voltage Low	IOHV_OD	ILOAD = 4mA	0		0.5	V

Table 12 – Pins IO[5:1] and pin IOHV electrical parameter

6.3.7. LIN related parameters

The LIN related parameters ISO_DIS_17987-4 , SAE J2602 with 8V ≤ VBAT ≤ 18V.

Parameter	Symbol	Conditions	min	typ	max	Unit
Transmitter DC Parameters						
Short circuit bus current	IBUS_LIM	VBUS = VBAT, driver on	40		200	mA
Pull up resistance bus, normal mode	RSLAVE		20		60	kΩ
Pull up current, SLEEP MODE	ILIN_PU-Sleep	VBUS=0, VBAT=12V, SLEEP MODE	-100			µA
Input Leakage at the receiver incl. PU	IBUS_PAS_dom	VBUS=0, VBAT=12V, SLEEP MODE	-1			mA
Bus reverse current, recessive	IBUS_PAS_rec	driver off, 8V<VBAT<18V, 8V<VBUS<18V, VBUS > VBAT			20	µA
Bus reverse current loss of battery	IBUS_NO_BAT	VS = 0V, 0V < VBUS < 18V			23	µA
Bus current during loss of ground	IBUS_NO_GND	VS = VGND=12V, 0 < VBUS < 18V	-1		1	mA
Transmitter dominant voltage	VolBUS	network load =500Ω / TxDx = 0	0		0.2	VS

Parameter	Symbol	Conditions	min	typ	max	Unit
Transmitter recessive voltage	VohBUS	TxDx open	0.8		1	VS
BUS input capacitance; MLX Value for LIN conformance test [32]	CBUS	Pulse response via 10kΩ, VPULSE = 12V, VS open		25	35	pF
Receiver DC Parameters						
Receiver dominant voltage	VBUSdom				0.4	VS
Receiver recessive voltage	VBUSrec		0.6			VS
Centre point of receiver threshold	VBUS_CNT	$VBUSCNT=\frac{VBUSdom+VBUSrec}{2}$	0.475	0.5	0.525	VS
Receiver hysteresis	VBUS_hys	$VBUSCNT=\frac{VBUSdom+VBUSrec}{2}$			0.175	VS
AC Parameters						
Propagation delay receiver [26] [27] [28]	trx_pdf	CRxD =25pF falling edge			6	µs
Propagation delay receiver [26] [27] [28]	trx_pdr	CRxD =25pF rising edge			6	µs
Propagation delay receiver symmetry [28]	trx_sym	trx_pdf - trx_pdr	-2		2	µs
Receiver debounce time [29]	trec_deb	LIN rising & falling edge	0.5		4	µs
LIN duty cycle 1 [27] [30]	D1	19.8k baud operation , normal mode	0.396			
LIN duty cycle 2 [27] [30]	D2	19.8k baud operation , normal mode			0.581	
LIN duty cycle 3 [27] [30]	D3	10.4k baud operation , low speed mode	0.417			
LIN duty cycle 4 [27] [30]	D4	10.4k baud operation , low speed mode			0.590	
trec(max) – tdom(min) [31]	Δt3	10.4k baud operation , low speed mode			15.9	µs
trec(min) – tdom(max) [31]	Δt4	10.4k baud operation , low speed mode			17.28	µs
TxD dominant time out [32]	tTxD_to	normal mode, VTxD = 0V		32		ms
WAKE UP filter time pin LIN	tWU_LIN	Time for dominant level after SLEEP MODE	30		150	µs

Table 13 – LIN related parameters

26 *This parameter is tested by applying a square wave signal to the LIN. The access to internal signals RxD and TxD was made in a chip test mode. The minimum slew rate for the LIN rising and falling edges is 50V/µs*
27 *See LIN timing diagram*
28 *Parameter in relation to internal signal TxD*
29 *Internal MLX value to suppress spikes; only proved during characterization: not measured in production*
30 *Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal termination disabled*
31 *In accordance to SAE J2602*
32 *Guaranteed by design & characterization, not measured in production*

Baud rate	19.8k baud	10.4k baud
tBit	50µs	96µs
Dwc1	D1	D3
Dwc2	D2	D4
THREC(MAX)	0.744 VS_TX	0.778 VS_TX
THDOM(MAX)	0.581 VS_TX	0.616 VS_TX
THREC(MIN)	0.422 VS_TX	0.389 VS_TX
THDOM(MIN)	0.284 VS_TX	0.251 VS_TX

As shown in , a worst case duty cycles can be calculated:
Dwc1 = tBUS_rec(min) / 2 * tBit
Dwc2 = tBUS_rec(max) / 2 * tBIT
Thresholds for duty cycle calculation in accordance to LIN2.x:

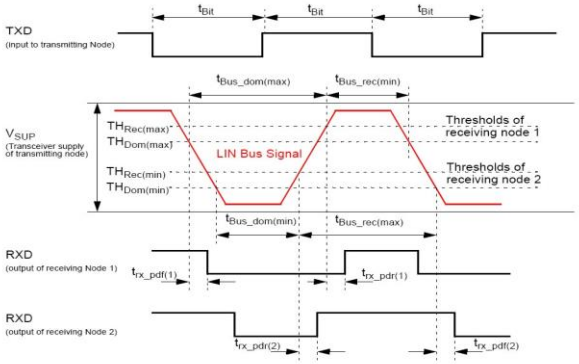


Figure 9. LIN timing diagram: Relation between propagation delay and duty cycle

6.3.8. FET Driver Electrical Parameter

Parameter	Symbol	Condition	min	typ	max	Unit
HS0/1/2, VS=13V, VREF_SEL=0						
Output on resistance for logic low measured between HS0/1/2 and U/V/W	RONHSL	T= -40°C,	3	8	30	Ω
		T= 35°C,	5	11	30	Ω
		T= 150°C,	6	16	30	Ω
Output on resistance for logic high measured between HS0/1/2 and CP0/1/2	RONHSH	T= -40°C,	5	13	40	Ω
		T= 35°C,	5	16	40	Ω
		T= 150°C,	5	22	40	Ω
LS0/1/2, VS=13V, VREF_SEL=0						
Output on resistance for logic low measured between LS0/1/2 and GND	RONLSL	T= -40°C,	5	8	30	Ω
		T= 35°C,	7	11	30	Ω
		T= 150°C,	12	16	30	Ω
Output on resistance for logic high measured between LS0/1/2 and VREF	RONLSH	T= -40°C,	8	13	40	Ω
		T= 35°C,	11	16	40	Ω
		T= 150°C,	15	22	40	Ω
Internal Interlock Delay						
minimum required internal interlock high-side driver	tILD_HS		150			ns
minimum required internal interlock low-side driver	tILD_LS		150			ns

Table 14 – FET driver electrical parameter

6.3.9. FET Drain Source Monitoring

Parameter	Symbol	Condition	min	typ	max	Unit
HS VDS 4 bit DAC						
Reference voltage	VREFHS_VDS_DAC		2.45	2.5	2.55	V
Differential nonlinearity	DNLHS_VDS_DAC	Only characterized.	-1		+1	LSB
HS_DS comparator						
Propagation delay high-side VDS monitoring comparator until IRQ occurs	TpdHSDS_CMP	Fclk=40MHz, Only characterized. For information only.	75	130	200	ns
LS VDS 4 bit DAC						
Reference voltage	VREFLS_VDS_DAC		2.45	2.5	2.55	V
Differential nonlinearity	DNLLS_VDS_DAC	Only characterized.	-1		+1	LSB
LS_DS comparator						
propagation delay low-side VDS monitoring comparator until IRQ occurs	TpdLSDS_CMP	Fclk=40MHz, Only characterized. For information only.	75	130	200	ns

Table 15 – FET Drain Source Monitoring Parameter

7. Functional Description

7.1. Block Diagram

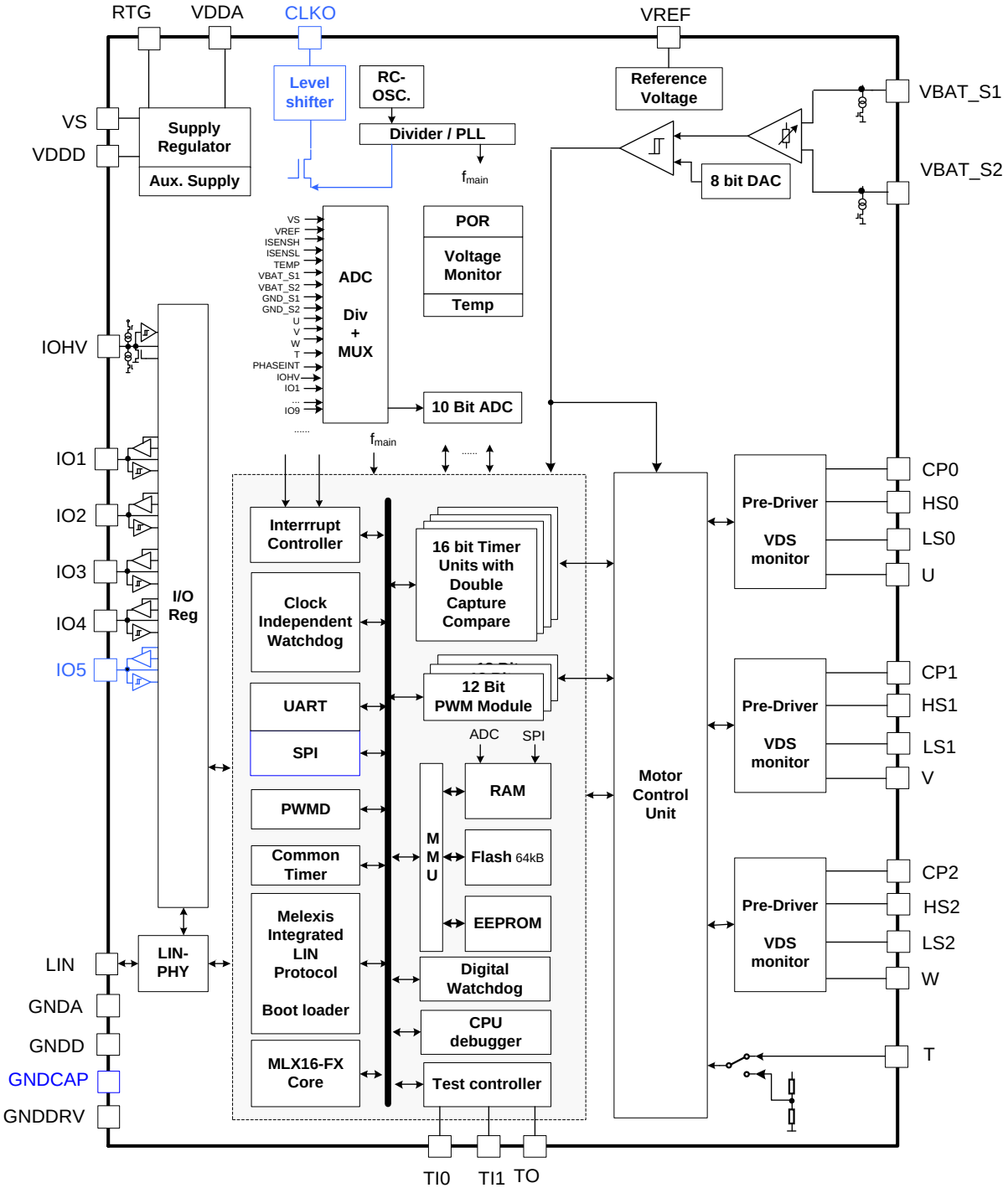


Figure 10. Block Diagram

Colour legend:
Black: common for MLX81206 and MLX81208
Blue: additional pins or functionality for MLX81208

8. ESD and EMC

In order to minimize EMC influences, the PCB has to be designed according to EMC guidelines. The MLX81206/08 are ESD sensitive devices and have to be handled according to the rules of IEC61340-5-2. MLX81206/08 will apply the requirements in the application according to the specification and to ISO7637-2, -3.
Prototype samples of MLX81206/08 will be evaluated according AEC-Q100. The result will be published after qualification. After ESD stress single parameters may be shifted out of their limit, but IC function will still be correctly.

8.1. Automotive Qualification Test Pulses according to ISO7637-2/3 and ISO16750-2

Automotive test pulses are applied to module in an application environment and not to the single IC. Only protected pins (protection by means of the IC itself or by means of external components) are wired to module connectors. In the recommended application diagrams, the reverse polarity diode together with the capacitors on supply pins, the protection resistors in several lines and the load dump protected IC itself will protect the module against the below listed automotive test pulses. The exact value of the capacitors for an application has to be determined during design-in of the product according to the automotive requirements.

For the LIN pin the specification “LIN Physical Layer Spec 2.1 (Nov. 24, 2006)” is valid.
Supply Pin VS is protected via the reverse polarity diode and the supply capacitors. No damage will occur for defined test pulses. A deviation of characteristics is allowed during pulse 1 and 2; but the module will recover to the normal function after the pulse without any additional action. During test pulse 3a, 3b, 5 the module will work within characteristic limits.

8.1.1. **Test Pulses On supply Lines (directly connected to Car Battery)**

Parameter	Symbol	min	max	unit	test condition, functional state
Transient test pulses according to ISO7637-2 (supply lines) , VS=13.5V, TA=(23 ± 5)°C & (Document: “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications”; Audi, BMW, Daimler, Porsche, VW; 2009-12-02)					
Test pulse #1	vpulse1	-100		V	5000 pulses, functional state C
Test pulse #2	vpulse2		50	V	5000 pulses, functional state A
Test pulse #3a	vpulse3a	-150		V	1h, functional state A
Test pulse #3b	vpulse3b		100	V	1h, functional state A
Transient test pulses in according to ISO16750-2 , VS=13.5V, TA=(23 ± 5)°C					
Test pulse #5b	vpulse5b	65	87	V	1 pulse clamped to 27V (+13V (VS)), (32V (+13V (VS))for applications for north America), functional state C

Table 16 – Test pulses Supply Line

8.1.2. Test pulses on LIN Lines

Parameter	Symbol	min	max	unit	Coupling	test condition, functional status
Transient test pulses in accordance to ISO7637-3, VS=13.5V, TA=(23 ± 5)°C & (Document: "Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications"; Audi, BMW, Daimler, Porsche, VW; 2009-12-02)						
Test pulse 'DCC slow –'	Vpulse_ slow+	-100		V	Direct capacitive coupled: 1nF	1000 pulses, functional state D
Test pulse 'DCC slow +'	Vpulse_ slow-		75	V	Direct capacitive coupled: 1nF	1000 pulses, functional state D
Test pulse 'DCC fast a'	Vpulse_ fast_a	-150		V	Direct capacitive coupled: 1nF	10 min, functional state D
Test pulse 'DCC fast b'	Vpulse_ fast_b		100	V	Direct capacitive coupled: 1nF	10 min, functional state D

Table 17 – Test pulses LIN

8.1.3. Test pulses on signal lines

Parameter	Symbol	Min	Max	Dim	Coupling	test condition, functional status
Transient test pulses in accordance to ISO7637-3 (signal lines). VS=13.5V, TA=(23 ± 5)°C						
Test pulse 'DCC slow –'	Vpulse_ slow-	-30	-8	V	Direct capacitive coupled: 100nF	1000 pulses, functional state C
Test pulse 'DCC slow +'	Vpulse_ slow+	+8	+30	V	Direct capacitive coupled: 100nF	1000 pulses, functional state A
Test pulse 'DCC fast a'	Vpulse_ fast_a	-60	-10	V	Direct capacitive coupled: 100pF	10 min, functional state A
Test pulse 'DCC fast b'	Vpulse_ fast_b	10	40	V	Direct capacitive coupled: 100pF	10 min, functional state A

Table 18 – Test pulses signal lines

Description of functional states

A: All functions of the module are performed as designed during and after the disturbance.

B: All functions of the module are performed as designed during and after the disturbance: However one or more can go beyond specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain class A.

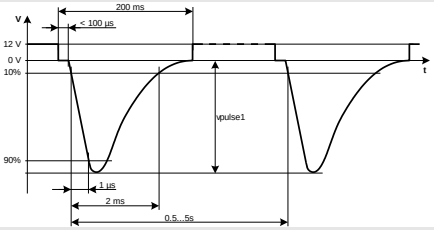
C: A function of the module is not performed as designed during disturbance but returns automatically to a normal operation after the disturbance

D: A function of a device does not perform as designed during the disturbance occurs and does not return automatically to the normal operation after the disturbances is removed. The device needs to be reset by a simple operation/action to return to the specified limits/function.

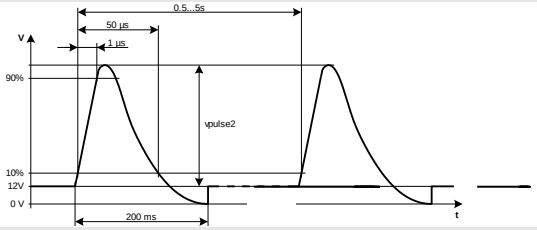
8.1.4. EMV Test pulse definition

EMV Test Pulse shapes (ISO7637-2 (supply lines))

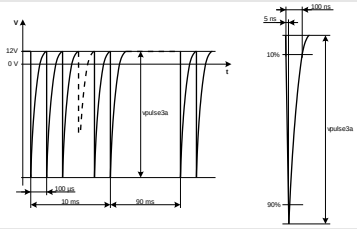
Test Pulse 1
Ri = 10 Ω



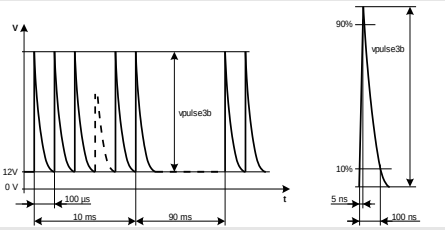
Test pulse 2
Ri = 2 Ω



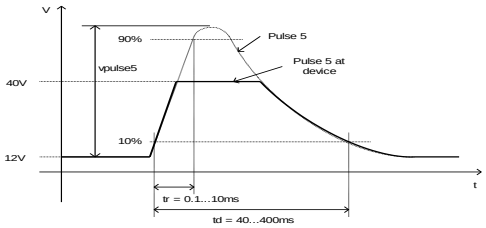
Test Pulse 3a
Ri = 50 Ω



Test Pulse 3b
Ri = 50 Ω

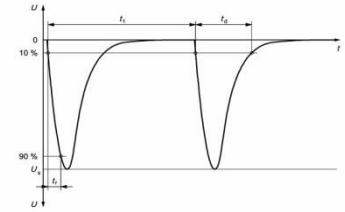


Test Pulse 5 (Load Dump)
Ri = 0.5…4 Ω (clamped to 45V during test)



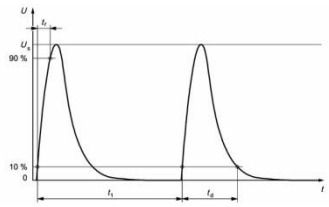
EMV Test Pulse shapes (ISO7637-3 (non-supply lines))

Test Pulse 'DCC slow -'
Ri = 2 Ω



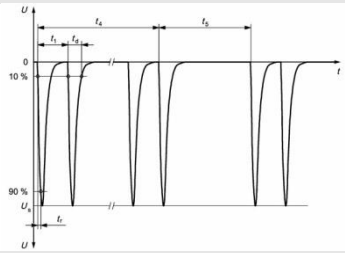
Parameters	
U_s	To be defined in test plan
t_r	⩽1 µs
t_d	0,05 ms
t_1	0,5 s to 5 s
R_i	2 Ω

Test pulse 'DCC slow +'
Ri = 2 Ω



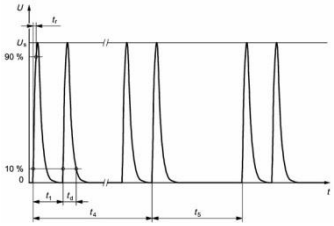
Parameters	
U_s	To be defined in test plan
t_r	⩽1 µs
t_d	0,05 ms
t_1	0,5 s to 5 s
R_i	2 Ω

Test Pulse 'Fast a, DCC'
Ri = 50 Ω



Parameters	12 V system
U_s in V	See Table B.1
t_r in ns	5
t_d in µs	0,1
t_1 in µs	100
t_4 in ms	10
t_5 in ms	90
R_i in Ω	50

Test Pulse 'Fast b, DCC'
Ri = 50 Ω



Parameters	12 V system
U_s in V	See Table B.1
t_r in ns	5
t_d in µs	0,1
t_1 in µs	100
t_4 in ms	10
t_5 in ms	90
R_i in Ω	50

8.1.5. Typical Application Circuitry

In order to minimize EMC influences, the external application circuitry shall be designed as followed:

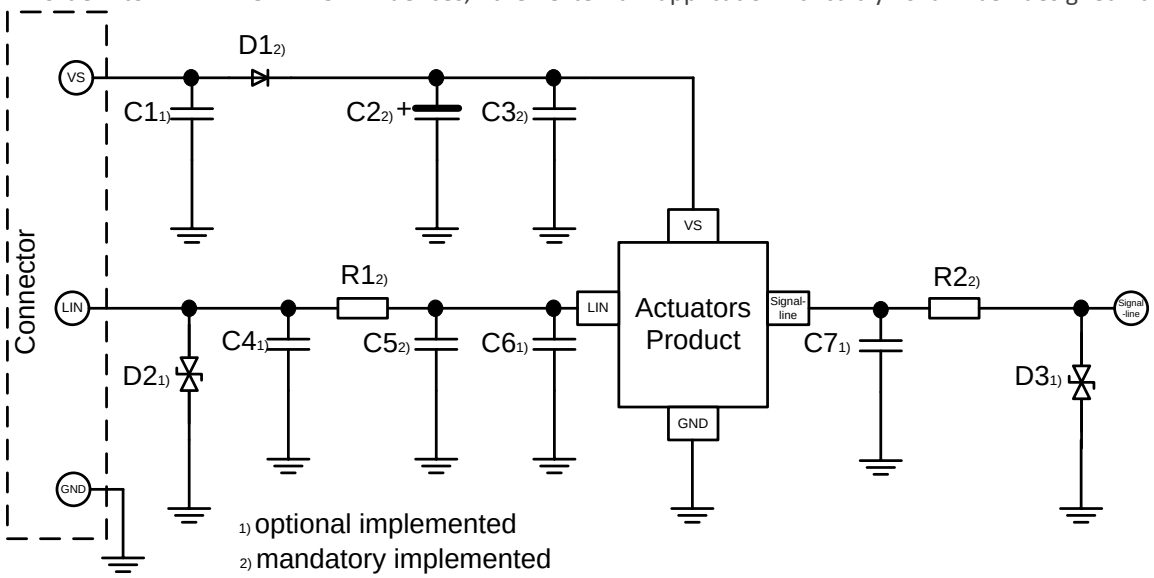


Figure 11. External application circuitry

8.1.5.1. External Circuitry on Supply Lines

In order to minimize EMC influences, the external application circuitry shall be designed as followed:

Name	Mounting	Min	Recommended	Max	Dim	Comment
C1	recommended	-	100	-	nF	Ceramic SMD: 10%, 0805, ≥50V; close to the connector
D1	mandatory					Inverse-polarity protection diode
C2	mandatory	1	22	100	µF	Tantal SMD: 10%, 7343, 35V
C3	mandatory	-	100	-	nF	Ceramic SMD: 10%, 0805, ≥50V; close to the pin

8.1.5.2. External Circuitry on LIN Lines

In order to minimize EMC influences, the external application circuitry shall be designed as followed:

Name	Mounting	Min	Recommended	Max	Dim	Comment
D2	no	-	PESD1LIN	-		ESD protection Diode: SOD323 close to the connector; optional part
C4	no	-	-	-	pF	Ceramic SMD: 10%, 0805, ≥50V; $C_{Slave} \leq C_{D2}+C_4+C_5+C_6+C_{IC}$ $C_{Slave} \leq 250pF$; optional part
R1	mandatory	-	0	-	Ω	Serial resistor: 0805;or optional Ferrite
C5	mandatory	-	220	-	pF	Ceramic SMD: 10%, 0805, ≥50V; $C_{Slave} \leq C_{D2}+C_4+C_5+C_6+C_{IC}$ $C_{Slave} \leq 250pF$
C6	no	-	-	-	pF	Ceramic SMD: 10%, 0805, ≥50V; $C_{Slave} \leq C_{D2}+C_4+C_5+C_6+C_{IC}$ $C_{Slave} \leq 250pF$; optional part

8.1.5.3. External Circuitry on Signal Lines

In order to minimize EMC influences, the external application circuitry shall be designed as followed:

Name	Mounting	Min	Recommended	Max	Dim	Comment
C7	no	0.1	1	100	nF	Ceramic SMD: 10%, 0805, ≥50V; optional part
R2	mandatory	0	560	1000	Ω	Serial resistor: 0805; or optional Ferrite
D3	no	-	PESD1LIN	-		ESD protection Diode: SOD323 close to the connector; optional part

9. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solder ability and moisture sensitivity level according to following test methods:

Reflow Soldering SMDs (Surface Mount Devices)

IPC/JEDEC J-STD-020
Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices
(Classification reflow profiles according to table 5-2)
EIA/JEDEC JESD22-A113
Preconditioning of Non-hermetic Surface Mount Devices Prior to Reliability Testing
(Reflow profiles according to table 2)

Wave Soldering SMDs (Surface Mount Devices) and THDs (Through Hole Devices)

EN60749-20
Resistance of plastic- encapsulated SMDs to combined effect of moisture and soldering heat
EIA/JEDEC JESD22-B106 and EN60749-15
Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THDs (Through Hole Devices)

EN60749-15
Resistance to soldering temperature for through-hole mounted devices

Solder ability SMDs (Surface Mount Devices) and THDs (Through Hole Devices)

EIA/JEDEC JESD22-B102 and EN60749-21

Solder ability
For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMDs is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/Quality_soldering.aspx) as well as trim&form recommendations (http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx).

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

10. Document History

Vers.	IC revision	Date	Author	Changes
V 1.0	MLX81206/08	25-March-2019	MLB	Initial product abstract, based on datasheet MLX81206/08 V1.1
V 1.1	MLX81206/08	13-May-2020	FJE	Updated order codes and package info, based on datasheet MLX81206/08 V1.4
V 1.2	MLX81206/08	04-May-2023	FJE	Updated Table 13, based on datasheet MLX81206/08 V1.6 Updated disclaimer

11. Contact

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