1. Features and benefits

- Motor driver
  - 6x Driver for external relays, or 6x Pre-Driver for external PN-FET half-bridges up to 30nC with 6x PWM
- Microcontroller:
  - MLX16-FX, application CPU
  - MLX4, communication CPU
  - Programmable digital watch-dog
  - Interrupt controller
  - Common purpose timer
- Memories split per CPU
  - MLX16-FX memories:
    - 32 KB Flash with ECC
    - 10 KB ROM
    - 2 KB RAM
    - 512 B EEPROM
  - MLX4 memories:
    - 6 KB ROM
    - 512 B RAM
- Fast end-of-line programming via LIN pin (32 KB Flash in < 2.5sec)
- Compatible SW for motor IC family
    - MLX81160: 48 KB PN-FET driver
    - MLX81344: 90 KB NN-FET driver
- Periphery
  - Configurable RC-clock 12MHz to 32MHz
  - 12x general purpose IO's, up to 9x high-voltage analog inputs, 2x UART, SPI, I^2C-slave
  - 6x 16-bit motor PWM timers
  - 2x 16-bit timers
  - 12-bit ADC with < 1.2µs conversion time with 32 channels
  - 2x Differential current sense amplifier with 8-bit programmable overcurrent
  - Temperature sensor, over-temperature detection
  - Over-current detection, over-voltage and under-voltage protection
- Voltage regulators
  - Internal voltage regulators, directly powered from 12V battery supply
  - IC operating motor voltage VSM = 5.5V to 32V* (*operating voltage up to 38V limited to 24h over lifetime)
  - Operating voltage VS = 5.5V to 32V* (*operating voltage up to 38V limited to 24h over lifetime)
  - Operation down to 3.5V with reduced analog characteristics, down to 3.0V without losing register content, down to 1.6V with intact RAM memory
  - Low standby current consumption of typ 25µA in sleep mode
  - Wake-up possible via LIN, external pins or internal wake-up timer
- Bus interface
  - LIN 2.x/SAE J2602 and ISO17987-4 compliant LIN slave
- Package QFN24 4x4 WF
- **Automotive AEC-Q100 qualified**

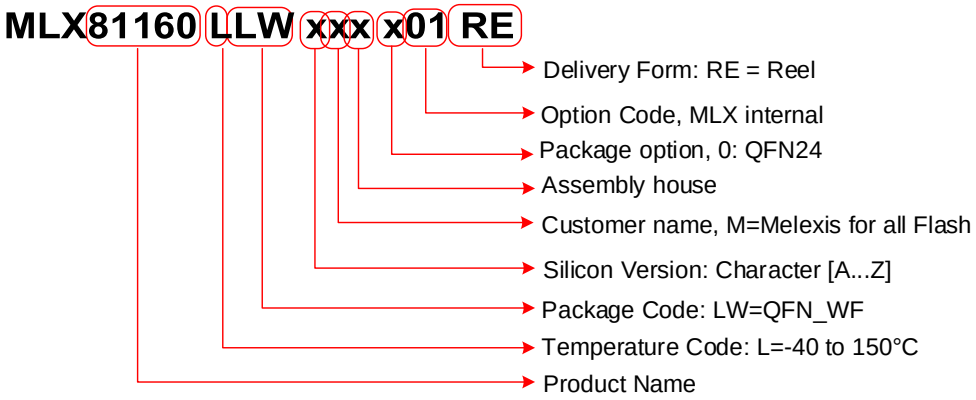
2. Application examples

- DC Window Lift, Sunroof with Relays or PN-MOSFETs
- DC/BLDC pump or fan with PWM-drive and PN-MOSFETs
- Multiple small DC motors with PN-MOSFETs

3. Ordering information

Order Code	Temp. Range	Package	Delivery	Remark
MLX81160LLW-AMT-001-RE	-40 - 150 °C	QFN24_WF 4x4	Reel	6x Driver + 12x IO

Table 1 – Ordering Information



4. Family Concept

	MLX81160	MLX81344
MCU Memory	32 KB Flash + 16 KB ROM	64 KB Flash + 26 KB ROM
MCU EEPROM	64x 8 B	64x 8 B
MCU RAM	2.5 KB	4.5 KB
Pre-Driver	6x Relay drivers, or PN-MOSFET Predrivers	DC or BLDC N-MOSFET Predrivers
Motor Power range	typ. 200W	typ. 200W
Motor Voltage range	5.5V...38V	5.5V...36V
IO pins (analog, digital)	9x LV + 3x HV/LV	9x LV + 3x HV/LV
Motor current sensing	2x Low side shunt, Differential	Low side shunt, differential
Sensor interface (3V/5V supply)	analog, pwm, spi, sent, I^2C, uart	analog, pwm, spi, sent, I^2C, uart
Sensorless FOC support	Yes (BLDC motor)	Yes (BLDC motor)
Maximum IC Temperature (with validated mission profile)	T_j = 175°C	Tj = 175°C
Package	QFN24, 4x4	QFN32, 5x5 QFN24, 4x4
Automotive AECQ-100	Yes	Yes

Table 2 – Famiy Overview

5. Revision history

Version	Date	Description
1.0	01/10/2022	Initial MLX81160 product abstract

Table 3 – Revision history

6. Contents

7. System block diagram and system functions

The system block diagram is shown in Figure 1, where the key system functions of MLX81160 are illustrated, i.e. the capability to drive the phases of a motor over relays or PN-FET halfbridges, to read data from sensors and to communicate with the engine control unit (ECU) over a LIN compliant interface.

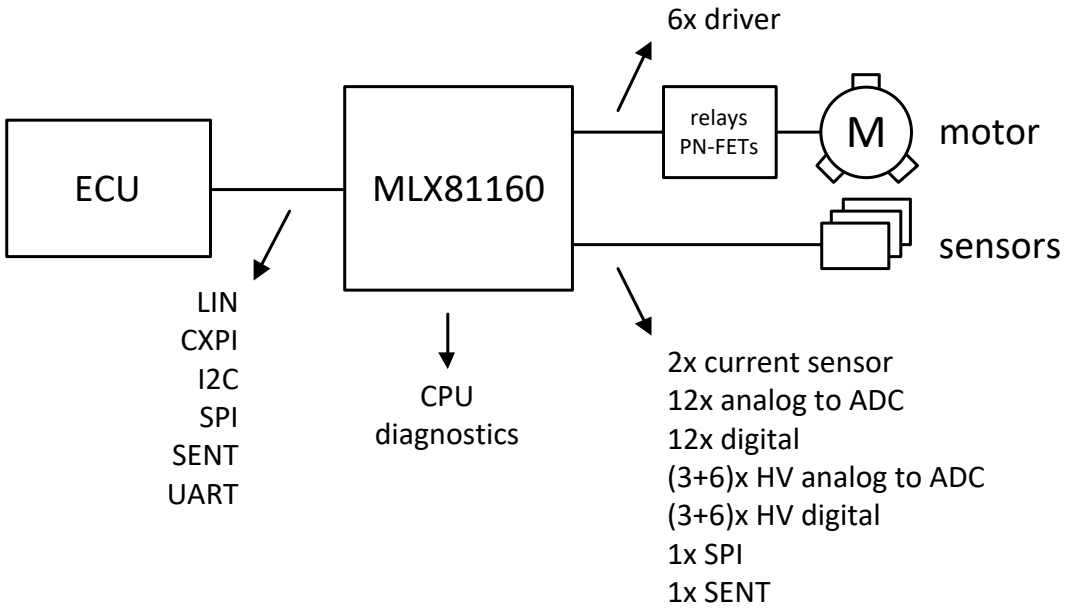


Figure 1 – System block diagram

The system functions of MLX8160 are:

- Motor driving:
  - The IC can drive up to 6 external relays
  - The IC can drive up to 6 external PN-FET half-bridges, up to 30nC gate charge to support motors ranging from 10W - 200W
  - The IC can process standard or complex motor drive algorithms like BEMF or FOC
- Sensing:
  - The IC can read the voltage over up to 2 external low-side current sense resistors.
  - The IC can read up to 12 analog outputs of external sensors.
  - The IC can receive up to 12 digital signals.
  - The IC can read up to 3 high-voltage analog levels.
  - The IC can receive up to 3 high-voltage digital signals.

- The IC can receive a high-voltage digital signal at up to 6 phase pins.
- The IC can receive as an I^2C master the output of an external sensor.
- The IC can receive as an SPI master the output of an external sensor.
- The IC can receive SENT data (SAE J2716) via an IO pin.
- The IC can provide a configurable 3.3V / 5V supply for external sensors.
- The IC can sense the motor supply voltage.
- The IC can sense the driver pin voltages.

- Communication:
  - The IC supports LIN 2.x, SAE J2602 and ISO17987-4 standards as a slave node
  - The IC supports CXPI (Clock eXtension Peripheral Interface, JASO D015, ISO20794-2, SAE J3076) with exception of CT056-4
  - The IC supports I^2C Standard-mode, Fast-mode and Fast-mode Plus as a master/slave node
  - The IC supports the SPI standard
  - The IC can transmit a digital SENT signal
  - The IC can read up to 3 high-voltage analog levels
  - The IC can read up to 3 high-voltage digital signals
  - The IC supports receiving and transmitting a PWM communication signal at the LIN pin
  - The IC supports receiving and transmitting up to 2 UART signals
  - The IC‘s sleep current is < 50µA.
  - The IC can wake-up from sleep mode.
  - The IC can perform a reset triggered by an external state transition of an IO pin (GPIO pin configurable as reset pin).

The diagnostic functions of the IC are covered in the safety manual.

8. Functional safety

The MLX81160 is an ASSP developed as SEooC [ISO 26262] with assumed technical safety requirements with ASIL-B capability targets. The technical safety concept is described in the MLX81160 Safety manual.

9. IC block diagram

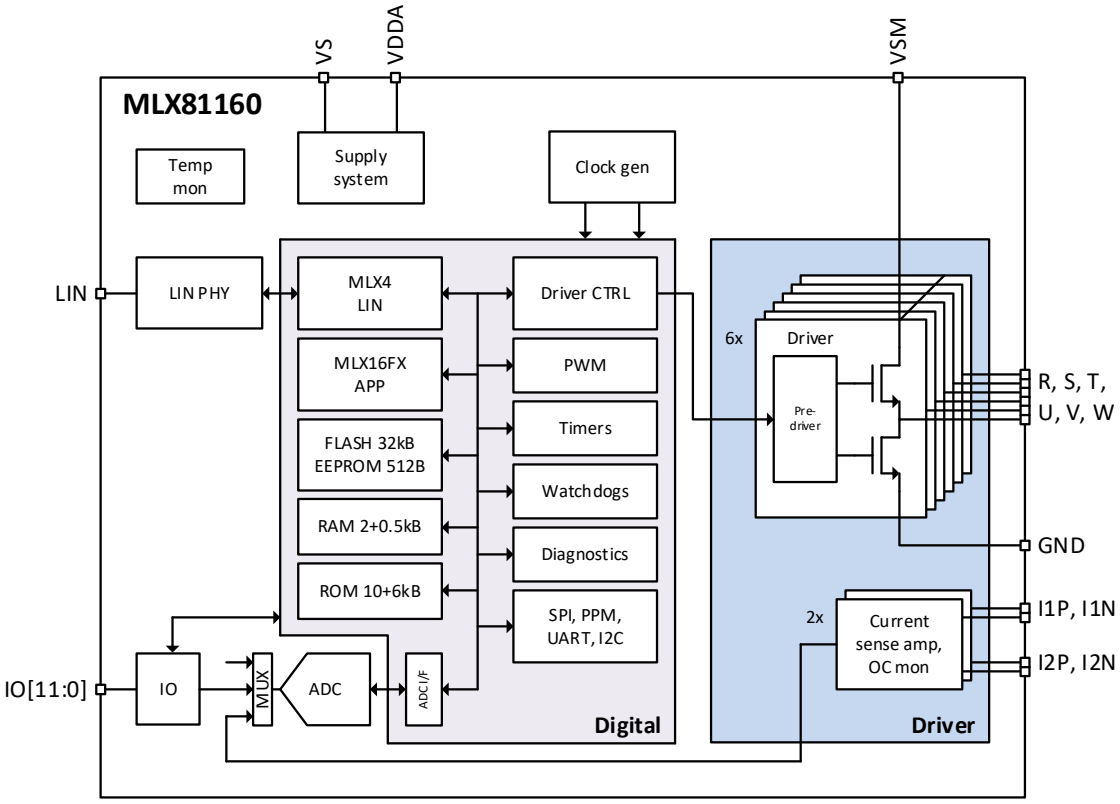


Figure 2 – IC Block diagram

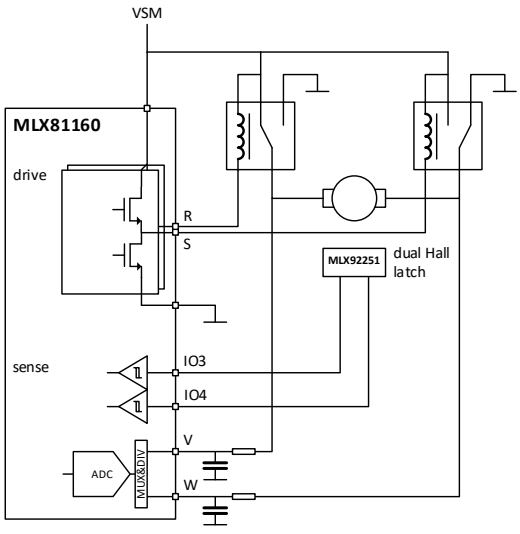


Figure 3 – Application example with relay

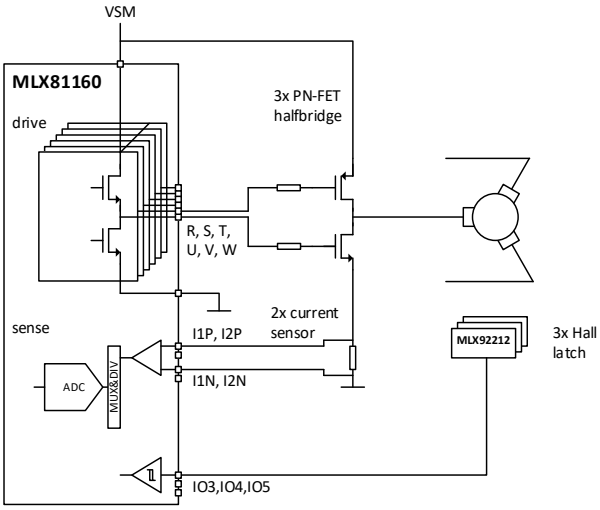
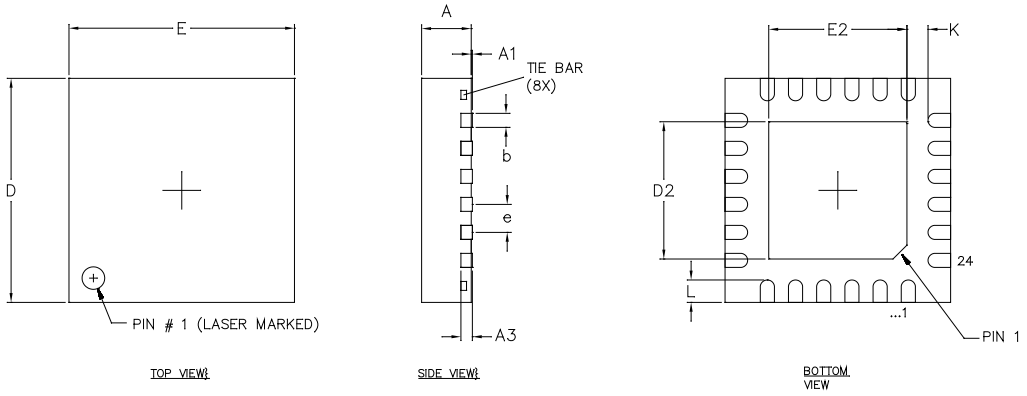


Figure 4 – Application example with PN-FET

10. Technical description

10.1. Package data QFN24



COMMON DIMENSIONS AND TOLERANCES

SYMBOL	ALL DIMENSION ARE IN MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.35	2.45	2.55
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
K	0.20		
b	0.18	0.25	0.30
e		0.50 BSC	

NOTE :
1. EXPOSED TIE BAR SHOULD BE KEPT FREE FROM SOLDER.
2. (OPTIONAL) SIDE WALL IMMERSION TIN PLATING MIN 1um THICK.

Figure 5 – Package data QFN24

10.2. Package pin-out

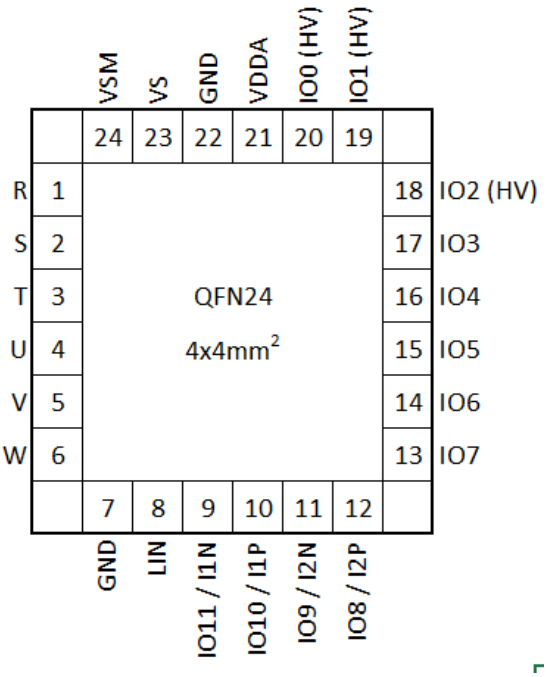


Figure 6 – Pin-out diagram QFN24 (-001 variant)

10.3. Pin-out description

Pin	Pin name	Description	Comment
QFN24, 4x4mm			
1	R	R-Phase Driver, or Pre-driver for PN-FET	
2	S	S-Phase Driver, or Pre-driver for PN-FET	
3	T	T-Phase Driver, or Pre-driver for PN-FET	
4	U	U-Phase Driver, or Pre-driver for PN-FET	
5	V	V-Phase Driver, or Pre-driver for PN-FET	
6	W	W-Phase Driver, or Pre-driver for PN-FET	
7	GND	GND Motor, GND Digital	
8	LIN	LIN interface pin	
9	IO11 / I1N	LVIO / Current sense input 1 (-)	
10	IO10 / I1P	LVIO / Current sense input 1 (+)	
11	IO9 / I2N	LVIO / Current sense input 2 (-)	
12	IO8 / I2P	LVIO / Current sense input 2 (+)	
13	IO7	LVIO + test output for development	option /reset pin
14	IO6	LVIO + test input for development	
15	IO5	LVIO	
16	IO4	LVIO	
17	IO3	LVIO	
18	IO2 (HV)	LVIO + HVIO	
19	IO1 (HV)	LVIO + HVIO	
20	IO0 (HV)	LVIO + HVIO	
21	VDDA	3.3V	3.3V IO supply, option 5V, for external sensors <25mA
22	GND	GND IC (analog)	
23	VS	Supply IC	
24	VSM	Supply Motor	

Table 4 – Pin-out description for QFN24

10.4. Marking instruction

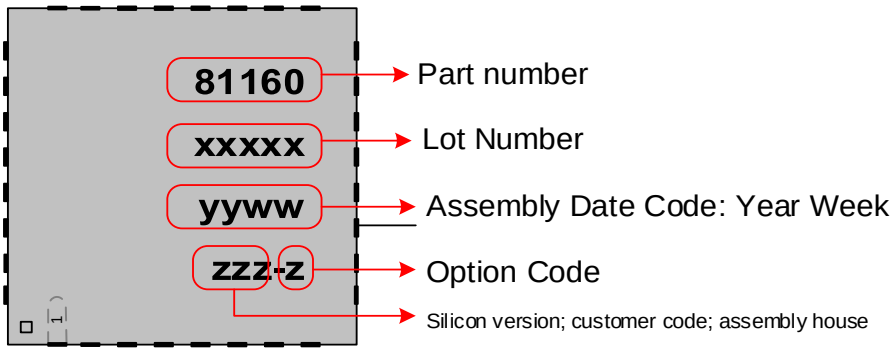


Figure 7 – Marking example on IC package QFN24 4x4 package

11. Typical application schematic

In the following schematic examples, external components are indicated that may be needed to protect the IC against EMC/ESD pulses. Depending on ECU conditioned power, over-voltage and reverse polarity discretes may be needed. Capacitor discretes depend on specific OEM ESD/EMC requirements.

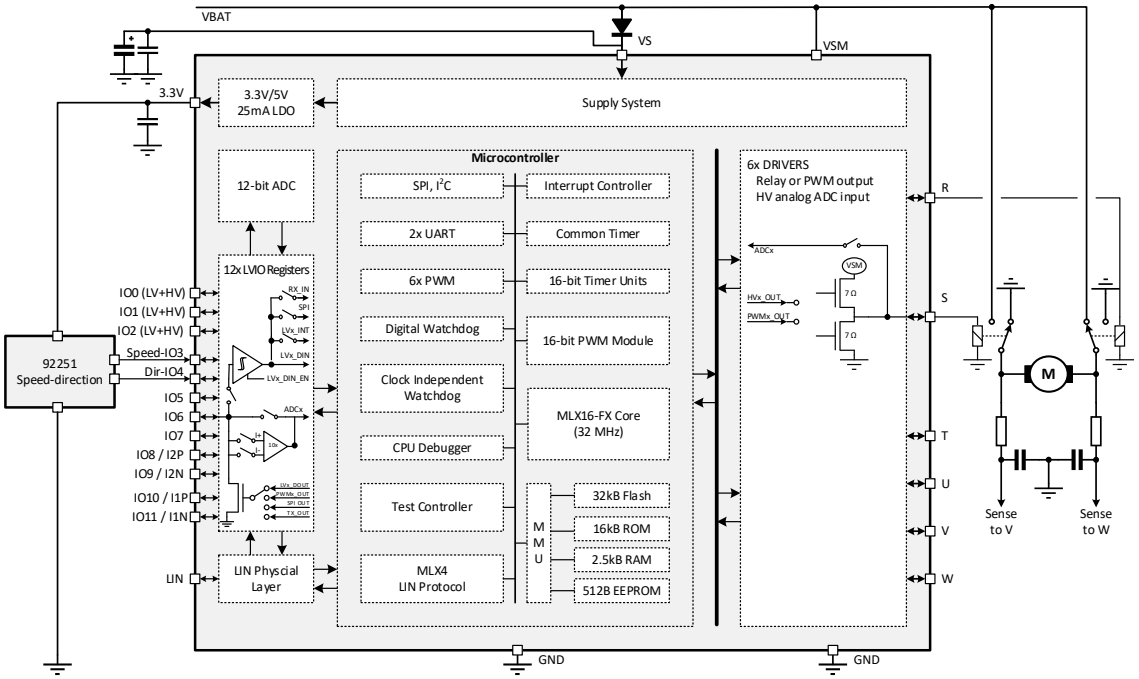


Figure 8 – DC Relay motor schematic with MLX81160 in QFN24

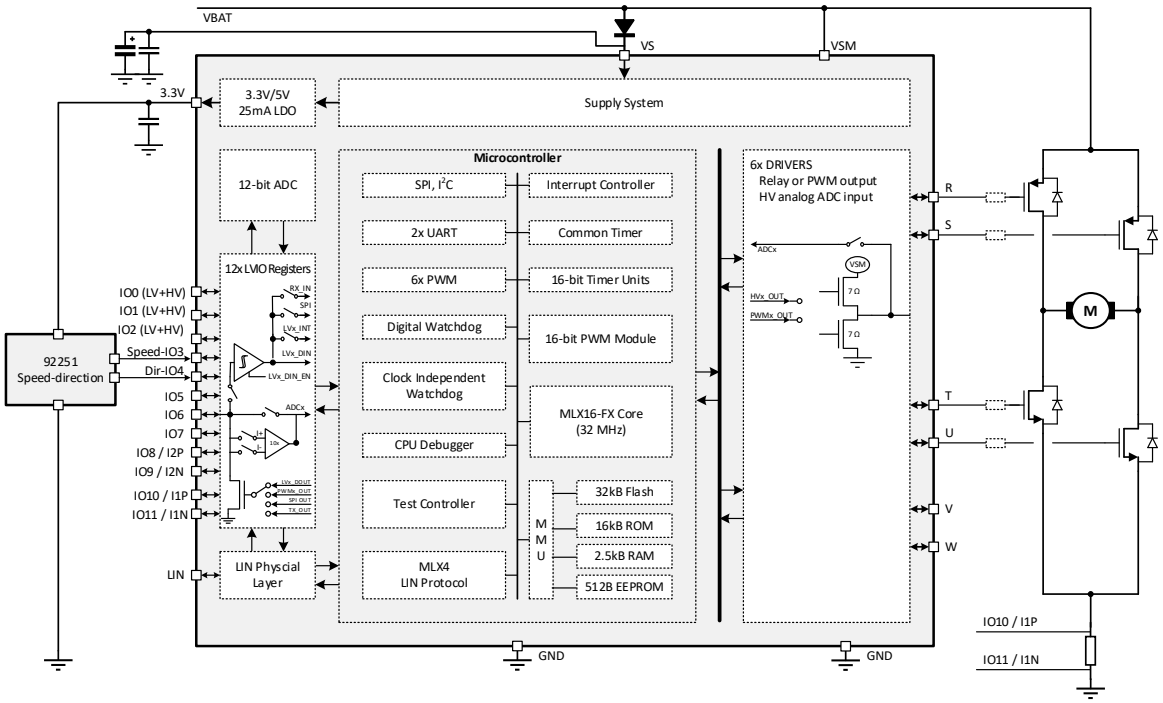


Figure 9 – DC motor with PN-MOSFET schematic with MLX81160 in QFN24

12. Electrical characteristics

12.1. Absolute maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage IC	VS	-0.5		32 38 [1]	V	
Supply voltage IC	VS	-0.5		45	V	t < 500ms
Supply voltage Motor	VSM	VDDA-0.3		32 38 [1]	V	
Supply voltage Motor	VSM	VDDA-0.3		45	V	t < 500ms
Supply voltage transient	VS.tr1	-100			V	ISO 7637-2 pulse 1 [2]
Supply voltage transient	VS.tr2			75	V	ISO 7637-2 pulse 2 [2]
Supply voltage transient	VS.tr3	-150		100	V	ISO 7637-2 pulses 3a, 3b [2]
Output voltage	VDDA	-0.3		5.5	V	
LIN bus voltage	VLIN	-40			V	Referenced to VS
LIN bus voltage	VLIN			40	V	Referenced to GND
LIN bus voltage transient	VLIN.tr1	-30			V	ISO 7637-3 DCC slow - [3]
LIN bus voltage transient	VLIN.tr2			30	V	ISO 7637-3 DCC slow + [3]
LIN bus voltage transient	VLIN.tr3	-150		100	V	ISO 7637-2 pulses 3a, 3b [3]
Phase pin voltage	VAN_PH	-0.3		VSM+0.3	V	R, S, T, U, V, W
Analog HV voltage	VAN_HV	-0.3		VS+0.3	V	IO0, IO1, IO2 (HV input mode)
Analog LV voltage	VAN_LV	-0.3		VDDA+0.3	V	IO0 to IO11
Current sense voltage	VAN_CS	-0.3		VDDA+0.3	V	I1P, I1N, I2P, I2N

[1] 38V operation is limited to maximum 24 hours over life
[2] ISO 7637 test pulses are applied to VS via a reverse polarity diode and blocking capacitor.
[3] ISO 7637 test pulses are applied to LIN via a coupling capacitance of 1nF.

Digital input voltage	VIN_DIG	-0.3		VDDA+0.3	V	IO0 to IO11
Digital output voltage	VOUT_DIG	-0.3		VDDA+0.3	V	IO0 to IO11
Reverse current into any IO	IREV_IO			1	mA	IO0 to IO11
Reverse current into all IO	IREV_IO_TOT			10	mA	IO0 to IO11
ESD HBM capability	ESD_HBM		+/-2		kV	All pins [4]
ESD HBM capability	ESD_HBM_LIN		+/-6		kV	Pin LIN. ESD applied on LIN pin versus shorted GND pins [4]
ESD CDM capability	ESD_CDM		+/-500		V	All pins [5]
Junction temperature	TJ	-55		175	ºC	
Thermal resistance, junction - ambient	RTH_JA		48		K/W	In free air [6]
Thermal resistance, junction - case	RTH_JC		7		K/W	[6]

Table 5 – Absolute maximum ratings

[4] *JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.*
[5] *JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.*
[6] *Valid for low thermal conductivity board (JEDEC).*

12.2. Operating range

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply voltage	VS	4	12	32	V	Analog full performance
Supply voltage	VS	3.5		4	V	Analog reduced performance [7]
Supply voltage	VS	32		38	V	Analog reduced performance [8]
Supply voltage	VS	3.0		32 38 [8]	V	Digital functional
Supply voltage	VS	1.6		32 38 [8]	V	SRAM content valid
Motor supply voltage	VSM	7		32 38 [8]	V	Driver full performance
Motor supply voltage	VSM	5.5		7	V	Driver reduced performance [9]
Junction temperature	T_J	-40		175	°C	

Table 6 – Operating range

[7] IC is functional down to 3.5V with reduced analog performance. During IC start-up, VS needs to be > 5.5V for a certain time to guarantee a correct reset. The VS range below 5.5V is only characterized. No production test.
[8] IC is functional up to 38V with reduced analog performance. 38V operation is limited to maximum 24 hours over life.
[9] Driver is functional at reduced performance (higher bridge resistance, reduced accuracy of current sense amplifier)

12.3. Electrical specifications

12.3.1. Current consumption

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Normal working current	INOM		10	15	mA	All IO pins are inputs; trimmed to 32 MHz; no external loads; no LIN communication; no ADC conversion
Sleep mode current	ISLEEP		25	50 100	µA	VS ≤ 18V, VSM ≤18V, Tj ≤ 150°C VS ≤ 32V, VSM ≤32V, Tj ≤ 150°C
Stop mode current	ISTOP		250	500	µA	
Holding mode current	IHOLD		7		mA	[10]

Table 7 – Electrical specifications: current consumption

12.3.2. Supply system

12.3.2.1. VDDA 3.3V regulator (including 5V option, external C: 0 … 220nF)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
3.3V analog supply voltage	VDDA	3.2	3.3	3.4	V	Bandgap and VDDA regulator trimmed
3.3V external current capability	IDDEXT_ VDDA	0		25	mA	VS ≥ 4V, external supply for sensors
3.3V under-voltage detection threshold	VTH_UV_ VDDA	2.75	2.85	2.95	V	VDDA ramping down
3.3V under-voltage detection hysteresis	VHYST_ UV_VDDA	0.1	0.175	0.25	V	
3.3V under-voltage debouncing time	TUV_ VDDA	1.0	3.0	10	µs	[10]
3.3V over-voltage detection threshold	VTH_OV_ VDDA	3.85	4	4.15	V	VDDA ramping up
3.3V over-voltage detection hysteresis	VHYST_ OV_VDDA	0.1	0.175	0.25	V	

[10] *No production test, guaranteed by design and verified during product verification*

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Over-voltage debouncing time	TOV_ VDDA	1.0	3.0	10	µs	[10]
Short detection threshold [11]	ISH_LH_ VDDA	40	65	90	mA	VS ≥ 4.5V (SWITCH_VDDA_TO_5V=0) VS ≥ 6V (SWITCH_VDDA_TO_5V=1)
Short detection hysteresis	IHYST_SH _VDDA	1.0	1.5	2.0	mA	[10]
5V option (SWITCH_VDDA_TO_5V=1)						
5V analog supply voltage (option)	VDDA5V	4.85	5	5.15	V	Bandgap and VDDA regulator trimmed
5V external current capability	IDDEXT_ VDDA5V	0		25	mA	VS ≥ 6V, external supply for sensors
5V under-voltage detection threshold	VTH_UV_ VDDA5V	4.05	4.2	4.35	V	VDDA ramping down
5V under-voltage detection hysteresis	VHY_UV_ VDDA5V	0.1	0.175	0.25	V	
5V over-voltage detection threshold	VTH_OV_ VDDA5V	5.6	5.8	6	V	VDDA ramping up
5V over-voltage detection hysteresis	VHY_UV_ VDDA5V	0.1	0.175	0.25	V	

Table 8 – Electrical specifications: VDDA regulator

12.3.2.2. VDDD 1.8V regulator

Parameter	Symbol	Min	Typ	Max	Unit	Condition
1.8V digital supply voltage	VDDD	1.80	1.875	1.95	V	Bandgap and VDDD regulator trimmed
1.8V current capability	IDDINT_ VDDD	15			mA	internal supply only, no external load; for information only

Table 9 – Electrical specifications: VDDD regulator

[11] ***Includes both internal and external current.***

12.3.2.3. VSM under-voltage and VSM over-voltage detection

Parameter	Symbol	Min	Typ	Max	Unit	Condition
VSM under-voltage detection threshold	VUV_LH_VS_0	3.5	4	4.5	V	Under-voltage detection on, PRUV_VS=0
VSM under-voltage detection threshold	VUV_LH_VS_1	4.5	5	5.5	V	Under-voltage detection on, PRUV_VS=1
VSM under-voltage detection threshold	VUV_LH_VS_2	5.5	6	6.5	V	Under-voltage detection on, PRUV_VS=2
VSM under-voltage detection threshold	VUV_LH_VS_3	6.5	7	7.5	V	Under-voltage detection on, PRUV_VS=3
VSM under-voltage detection threshold	VUV_LH_VS_4	7.5	8	8.5	V	Under-voltage detection on, PRUV_VS=4
VSM under-voltage detection threshold	VUV_LH_VS_5	8.5	9	9.5	V	Under-voltage detection on, PRUV_VS=5
VSM under-voltage detection hysteresis	VHYST_UV_VS	0.1	0.5	1	V	
VSM under-voltage debouncing time	TUV_VS	1.0	3.0	10	µs	[10]
VSM over-voltage detection threshold	VOV_LH_VS_0	16	18	20	V	Over-voltage detection on, PROV_VS=0
VSM over-voltage detection threshold	VOV_LH_VS_1	22	24	26	V	Over-voltage detection on, PROV_VS=1
VSM over-voltage detection threshold	VOV_LH_VS_2	38	40	42	V	Over-voltage detection on, PROV_VS=2
VSM over-voltage detection hysteresis	VHY_OV_VS	1	2	3	V	
VSM over-voltage debouncing time	TOV_VS	1.0	3.0	10	µs	[10]

Table 10 – Electrical specifications: VSM over- and under-voltage detection

12.3.2.5. Wake-up circuit

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Wake-up filter time IO pins	TWU_IO	15		80	µs	SLEEP mode , IO rising & falling edge
Wake-up filter time LIN pin	TWU_LIN	28		145	µs	Time for dominant level after SLEEP mode
Wake-up time internal timer	TWU_ INT_0		0			WUI=00 (no wake-up)
Wake-up time internal timer	TWU_ INT_1		$\frac{4096}{FRC\_10K}$			WUI=01 (~0.4s)
Wake-up time internal timer	TWU_ INT_2		$\frac{8192}{FRC\_10K}$			WUI=10 (~0.8s)
Wake-up time internal timer	TWU_ INT_3		$\frac{16384}{FRC\_10K}$			WUI=11 (~1.6s)

Table 11 – Electrical specifications: wake-up circuit

12.3.2.6. Bandgap

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Bandgap voltage	VBG	1.15	1.185	1.22	V	trimmed
Bandgap voltage temperature coeff.	TC_VBG	0		200	ppm/K	

Table 12 – Electrical specifications: bandgap

12.3.3. Clock generation

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Frequency 1MHz oscillator	FRC_1M	-5%	1	+5%	MHz	trimmed
Frequency 32MHz oscillator	FRC_32M	-5%	32	+5%	MHz	MCU clock: MCU_CLK info : 32MHz results in ~25 MIPS
Frequency 10kHz oscillator	FRC_10K	5	10	20	kHz	
Timing accuracy	TIMING_ ACC	-1.5		1.5	%	Timing accuracy after sw correction using EEPROM calibration values

Table 13 – Electrical specifications: clock generation

12.3.4. Motor driver module

12.3.4.1. Charge pump clock

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Charge pump clock frequency	FOSC_60	51	60	69	MHz	Trim value stored in EEPROM
Charge pump clock frequency	FOSC_82	71	82	93	MHz	Trim value stored in EEPROM (default)

Table 14 – Electrical specifications: driver clock

12.3.4.2. Output stage

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output peak current	I_OUTP		0.3		A	R, S, T, U, V, W peak current, when driving PN-FET halfbridge
Output current	I_OUTP			0.15	A	R, S, T, U, V, W dc current, when driving relay
High-side FET RDSon	R_HIGH		7	14	Ω	Top FET @ IC pin
Low-side FET RDSon	R_LOW		7	14	Ω	Bottom FET @ IC pin
Duty cycle range of PWM output	DC_OUT	5		95	%	For switching PWM (0% or 100% can be set as well) PWM frequency = 20kHz
Duty cycle of PWM output	DC_OUT	4		6	%	PWM duty cycle setting = 5% PWM frequency = 20kHz
Duty cycle of PWM output	DC_OUT	94		96	%	PWM duty cycle setting = 95% PWM frequency = 20kHz

Table 15 – Electrical specifications: output stage

12.3.5. Current sense amplifier

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input range	V_CSL_IR	-125		125	mV	Current sense range for CSA_HIGHGAIN = 0
Input range	V_CSH_IR	-62.5		62.5	mV	Current sense range for CSA_HIGHGAIN = 1
Amplifier gain	A_CSL	9.5	10	10.5		CSA_HIGHGAIN = 0
Amplifier gain	A_CSH	19	20	21		CSA_HIGHGAIN = 1
Low-pass filter time		0.25	0.5	1.0	µs	[10]
Over-current detection level	VTH_OC	10		300	mV	Programmable 8-bit DAC (1.56mV/LSB)
Over-current detection accuracy		-10		10	%	Full Scale VTH_OC range @VTH_OC 10mV…300mV for Tj<85˚ and @VTH_OC 200mV…300mV for Tj=(85˚..150˚)

Table 16 – Electrical specifications: current sense amplifier

12.3.6. VSM supply sensor

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Voltage range for ADC measurement				38	V	
VSM filter cut-off frequency				4	kHz	

Table 17 – Electrical specifications: VSM supply sensor

12.3.7. Over-temperature detection

Parameter	Symbol	Min	Typ	Max	Unit	Condition
OTD threshold	TTH_OT_LH	175	185	195	°C	Temperature ramping up
OTD threshold	TTH_OT_HL	150	160	170	°C	Temperature ramping down
OTD hysteresis	THY_OT	10	25		°C	

Table 18 – Electrical specifications: over-temperature detection

12.3.8. ADC

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Reference voltage	VREF_ADC		1.48		V	Trimmed and calibrated
Resolution			12		bit	ADC cyclic mode for differential input from -VREF_ADC to +VREF_ADC
Sample & Hold time				1	µs	
Conversion time	TCONV		1.125	1.18	µs	ADC_CLK= 16MHz
DNL		-1		1	LSB	[10]
INL		-3		3	LSB	
ADC channel accuracy - LV channels (with 1/2.5 divider)		-45		45	mV	0V – 3.3V input, calibrated acc. calibration document [12]
ADC channel accuracy - HV channels (with 1/26 divider		-0.30		0.30	V	<5V input, calibrated acc. calibration document
ADC channel accuracy - HV channels (with 1/26 divider)		-0.60		0.60	V	<20V input, calibrated acc. calibration document
ADC channel accuracy - VSMF channel (with 1/26 divider)		-0.20		0.20	V	<5V input, calibrated acc. calibration document
ADC channel accuracy - VSMF channel (with 1/26 divider)		-0.30		0.30	V	<20V input, calibrated acc. calibration document
ADC channel accuracy - temperature channel		-10		10	ºC	Calibrated acc. calibration document
ADC channel selection		0		63		

Table 19 – Electrical specifications: ADC

[12] *VS >= 4.5V for HVIO ADC LV channels IO[2:0]*

12.3.9. IOs

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input level L⇨H	VTH_LH			2.4	V	IO[11:0]
Input level H⇨L	VTH_HL	1			V	IO[11:0] [13]
Input hysteresis	VHY	0.1			V	IO[11:0]
LV output voltage L	VOL			0.4	V	IO[11:0] (LV-mode) ILOAD = 3mA
LV output voltage H	VOH	VDDA-0.4			V	IO[11:0] (LV-mode) ILOAD = 3mA
LV input range for ADC measurement		0		VDDA	V	IO[11:0] (LV-mode) Measurement of IO[11:0] / 2.5
HV output voltage L	VOL_HV			1.0	V	IO0, IO1, IO2 (HV-mode) ILOAD = 5mA
HV output voltage H	VOH_HV	VS-1.0			V	IO0, IO1, IO2 (HV-mode) ILOAD = 5mA
HV input range for ADC measurement		0		38	V	IO0, IO1, IO2 (HV-mode) Measurement of IOx/26
I2C SDA hold time (vs SCL)	TH_SDA	-50	0	50	ns	IO0 pin, SDAFILT_IO=00, setting for Fast-mode Plus
I2C SDA hold time (vs SCL)	TH_SDA	150	260	340	ns	IO0 pin, SDAFILT_IO=01
I2C SDA hold time (vs SCL)	TH_SDA	200	320	420	ns	IO0 pin, SDAFILT_IO=10
I2C SDA hold time (vs SCL)	TH_SDA	360	500	640	ns	IO0 pin, SDAFILT_IO=11, setting for Standard-mode and Fast-mode

Table 20 – Electrical specifications: IO

[13] *If an HV-IO is used as a global pin, then a series resistor of min. 390Ω / max. 10kΩ needs to be applied.*

12.3.10. LIN

12.3.10.1. LIN transceiver – static [14]

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Transmitter internal capacitance [10]	CLIN		30	40	pF	Response on 14V pulse via 1K
Bus short circuit current	IBUS_LIM	40		200	mA	VLIN = VS = 18V, VTxD = 0V
Pull up resistance bus	RSLAVE	20	35	60	kΩ	VDISTERM = 0
Pull up current bus, sleep mode	ISLAVE_ SLEEP	-50	-20	-5	µA	VLIN = 0V, VSBY = VAUX, VEN =0
Dominant input leakage current including pull up resistor	IBUS_PAS _dom	-1			mA	VLIN =0V, VS =12V, VTxD = VDDD, VDISTERM = 0 VEN = VDDD, VSBY = 0
Recessive input leakage current	IBUS_PAS _rec		0.25	20	µA	VEN = VDDD, VSBY = 0, VTxD = VDDD, VLIN > VS
Bus reverse current loss of battery [15]	IBUS_NO _BAT		0.25	23	µA	VS = 0V, 0V < VLIN ≤18V
Bus current during loss of ground [15]	IBUS_NO _GND	-100		1	µA	VS = VGND = 12V, 0 < VLIN ≤ 18V
Transmitter dominant output voltage [15]	VolBUS	0		0.2×VS	V	Rload = 500Ω
Transmitter recessive output voltage [15]	VohBUS	0.8× VS		1×VS	V	VEN = VDDD, VSBY = 0, VTxD = VDDD or sleep mode
Receiver dominant voltage	VBUSdom			0.4×VS	V	
Receiver recessive voltage	VBUSrec	0.6× VS			V	
Center point of receiver threshold	VBUS_ CNT	0.47 5×VS	0.5× VS	0.525× VS	V	VBUS_cnt = (Vth_dom+ Vth_rec)/2
Receiver hysteresis	VHYS			0.175× VS	V	VHYS = (Vth_rec –Vth_dom)

Table 21 – Electrical specifications: LIN transceiver – static (7V ≤ VS ≤ 18V)

[14] *Parameters are according to ISO17987-4, SAE J2602-1. Reduced performance for 5.5V < VS < 7V.*

[15] *In accordance to SAE J2602.*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Transmitter internal capacitance [14]	CLIN		30	40	pF	Response on 14V pulse via 1K
Bus short circuit current	IBUS_LIM	40		300	mA	VLIN = VS = 36V, VTxD = 0V
Pull up resistance bus	RSLAVE	20	35	60	kΩ	VDISTERM = 0
Pull up current bus, sleep mode	ISLAVE_SLEEP	-50	-20	-5	µA	VLIN = 0V, VSBY = VAUX, VEN =0
Dominant input leakage current including pull up resistor	IBUS_PAS_dom	-2			mA	VLIN =0V, VS =24V, VTxD = VDDD, VDISTERM = 0 VEN = VDDD, VSBY = 0
Recessive input leakage current	IBUS_PAS_rec		0.5	20	µA	VEN = VDDD, VSBY = 0, VTxD = VDDD, VLIN > VS
Bus reverse current loss of battery [15]	IBUS_NO_BAT		0.5	23	µA	VS = 0V, 0V < VLIN ≤ 36V
Bus current during loss of ground [15]	IBUS_NO_GND	-200		2	µA	VS = VGND = 12V, 0 < VLIN ≤ 36V
Transmitter dominant output voltage [15]	VolBUS	0		0.2×VS	V	Rload = 500Ω
Transmitter recessive output voltage [15]	VohBUS	0.8×VS		1×VS	V	VEN = VDDD, VSBY = 0, VTxD = VDDD or sleep mode
Receiver dominant voltage	VBUSdom			0.4×VS	V	
Receiver recessive voltage	VBUSrec	0.6×VS			V	
Center point of receiver threshold	VBUS_CNT	0.475×VS	0.5×VS	0.525×VS	V	VBUS_cnt = (Vth_dom+ Vth_rec)/2
Receiver hysteresis	VHYS			0.175×VS	V	VHYS = (Vth_rec –Vth_dom)

Table 22 – Electrical specifications: LIN transceiver – static (18V < VS ≤ 38V)

12.3.10.2. LIN transceiver – dynamic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Propagation delay receiver [16] [17]	trx_pdf			6	µs	CRxD =25pF falling edge
Propagation delay receiver [16] [17]	trx_pdr			6	µs	CRxD =25pF rising edge
Propagation delay receiver symmetry	trx_sym	-2		2	µs	Calculate trx_pdf - trx_pdr
Receiver debounce time	trx_deb	0.5		4	µs	LIN rising & falling edge
LIN duty cycle 1 [17] [18]	D1	0.396				20kbps operation, normal mode
LIN duty cycle 2 [17] [18]	D2			0.581		20kbps operation, normal mode
LIN duty cycle 3 [17] [18]	D3	0.417				10.4kbs operation, low speed mode
LIN duty cycle 4 [17] [18]	D4			0.590		10.4kbs operation, low speed mode
tREC(MAX) – tDOM(MIN) [19]	Δt3			15.9	µs	10.4kbs operation, low speed mode
tDOM(MAX) – tREC(MIN) [19]	Δt4			17.28	µs	10.4kbs operation, low speed mode
Slew rate on pin LIN normal mode, trimmed			1.2		V/µs	dV/dt between duty cycle measurement points, VS=12V
Slew rate on pin LIN low speed mode, trimmed			0.6		V/µs	dV/dt between duty cycle measurement points, VS=12V
TxD dominant timeout [20]	ttxd_to		15		ms	Normal mode, vTxD=0V

Table 23 – Electrical specifications: LIN transceiver – dynamic (7V ≤ VS ≤ 18V)

[16] *This parameter is tested by applying a square wave signal to the LIN. The minimum slew rate for the LIN rising and falling edges is 50V/µs.*
[17] *See Figure 10.*
[18] *Standard loads for duty cycle measurements are 1kΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal master termination disabled.*
[19] *In accordance to SAE J2602, see Figure 11.*
[20] *Parameter in relation to internal signal TxD.*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Propagation delay receiver [16] [17]	trx_pdf			6	µs	CRxD =25pF falling edge
Propagation delay receiver [16] [17]	trx_pdr			6	µs	CRxD =25pF rising edge
Propagation delay receiver symmetry	trx_sym	-2		2	µs	Calculate trx_pdf - trx_pdr
Receiver debounce time	trx_deb	0.5		4	µs	LIN rising & falling edge
LIN duty cycle 1 [17] [18]	D1	0.330				20kbps operation, normal mode
LIN duty cycle 2 [17] [18]	D2			0.642		20kbps operation, normal mode
LIN duty cycle 3 [17] [18]	D3	0.386				10.4kbs operation, low speed mode
LIN duty cycle 4 [17] [18]	D4			0.591		10.4kbs operation, low speed mode
tREC(MAX) – tDOM(MIN) [19]	Δt3			21.89	µs	10.4kbs operation, low speed mode
tDOM(MAX) – tREC(MIN) [19]	Δt4			17.47	µs	10.4kbs operation, low speed mode
Slew rate on pin LIN normal mode, trimmed			2.4		V/µs	dV/dt between duty cycle measurement points, VS=24V
Slew rate on pin LIN low speed mode, trimmed			1.2		V/µs	dV/dt between duty cycle measurement points, VS=24V
TxD dominant timeout [20]	ttxd_to		15		ms	Normal mode, vTxD=0V

Table 24 – Electrical specifications: LIN transceiver – dynamic (18V < VS ≤ 38V)

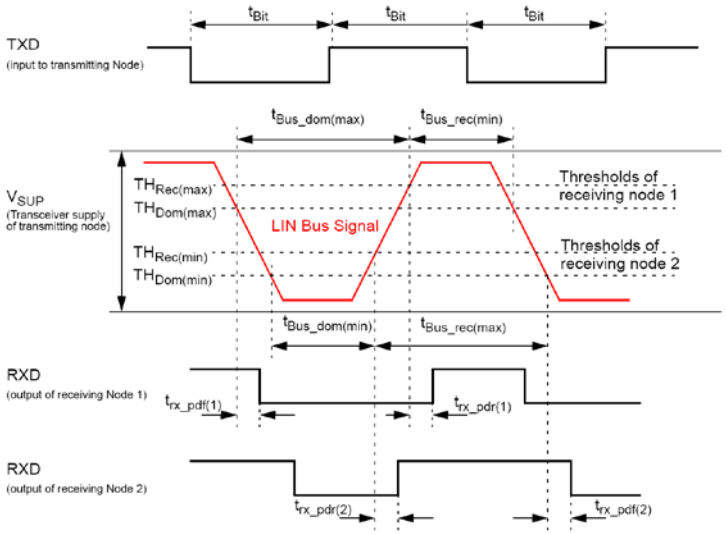


Figure 10 – LIN timing diagram (reference LIN2.1 specification)

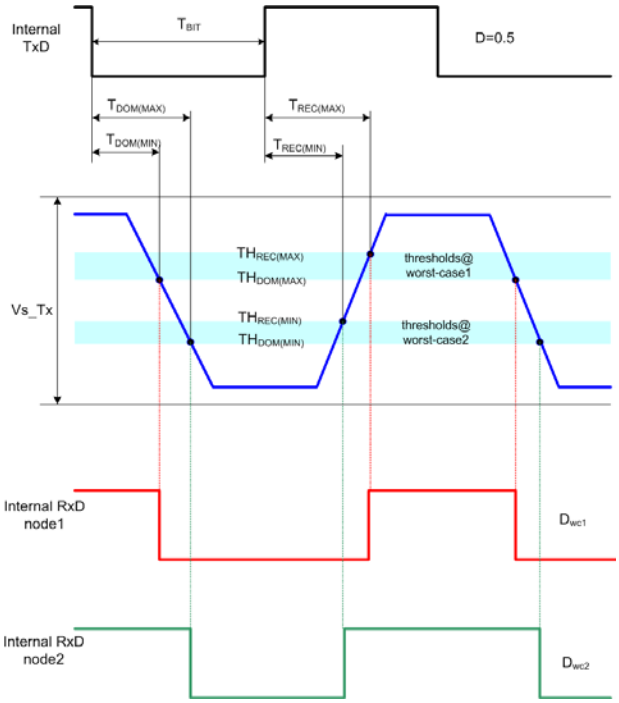


Figure 11 – LIN timing diagram, relation between propagation delay and duty cycle (reference SAE J2602 specification)

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