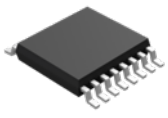
General description

Features and benefits

- Synchronized dual input channel readout
- High accuracy: maximum error ±0.36 °electrical for each inductive channel
- Immune to magnetic stray fields (ISO 11452-8)
- On-chip signal processing and latency compensation for enhanced accuracy and excellent dynamic behavior
- Flexible signal conditioning with 16-point programmable linearization characteristic per input channel
- External PWM channel readout
- On-chip differential and Vernier angle calculation
- Output interface SENT, SPC, PWM or SPI
- (fast) SENT according to SAE J2716 APR2016 featuring:
  - Enhanced serial data communication
  - Min. 0.5 µs tick time
- Overvoltage and reverse-polarity protection: -24 V to +24 V maximum
- Ambient Operating Temperature Range from -40 °C to 160 °C
- TSSOP-16 Package RoHS Compliant
- Compliant to ISO26262 with ASIL C(D)
- AEC-Q100 Qualified (Grade 0)



TSSOP-16

Application examples

- Torque sensor
- Steering angle sensor
- Torque and steering angle sensor
- High resolution rotary sensor
- High resolution linear sensor

Description

The MLX90514 is a dual input inductive position sensor suitable for automotive applications where the simultaneous measurement of two positions is required. The position information derived from the two channels can be directly transferred to the output or used for the calculation of derived quantities, in particular differential and Vernier angles. The MLX90514 is designed to control an inductive sensor system formed by the transmitting coil, one or two targets and two sets of receiver coils, each composed of three receiver coils. The on-chip LC oscillator generates an electromagnetic field together with the transmitting coil. This electromagnetic field induces, via the target(s), angle dependent voltages in the receiving coils. These signals are captured and processed by the MLX90514 internal DSP units according to the device configuration. The sensor is provided with an additional PWM input channel whose readout can also be used for the calculation of the derived quantities. The MLX90514 offers multiple output modes. It supports all standard formats of (fast) SENT and SPC including enhanced serial messages providing error codes. It can also be configured to output a PWM signal. For embedded applications, the SPI protocol allows fast protected data transfer and device programming.

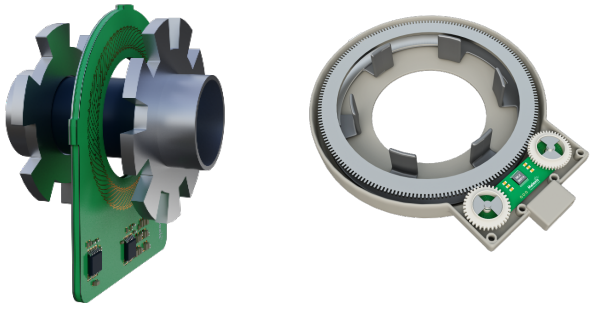


Figure 1: Application examples for torque sensing and steering angle sensing

Contents

1 Ordering information

Ordering Code	Temperature	Package	Definition	Packing
MLX90514GGO-AAA-100-RE	-40 °C to 160 °C	TSSOP-16	SENT/PWM/SPI output mode	Reel
MLX90514GGO-AAA-180-RE	-40 °C to 160 °C	TSSOP-16	SPC/SENT/PWM/SPI output mode	Reel

Table 1: Ordering codes

2 Glossary of terms

Term	Description
°el / °mech	Electrical / mechanical degree : °el = °mech · sensor periodicity
ABE	Analog Back-end
ADC	Analog-to-Digital converter
AGC	Automated gain control
AFE	Analog Front-end
AoU	Assumptions-of-Use
ASIL	Automotive Safety Integrity Level
CDM	Charge Device Model
CBD	Compensated By Difference (Angle)
DAC	Digital-to-Analog Converter
DC	Direct Current
DSP	Digital Signal Processing
EEPROM	Electrically Erasable Programmable Read Only Memory
ECU	Electronic Control Unit
EMC	Electro-Magnetic Compatibility
e-rpm	Electrical Revolutions per Minute. 1 e-rpm = 6 °el/s
ESD	Electro-Static Discharge
FDTI	Fault Detection Time Interval
FHTI	Fault Handling Time Interval
GCD	Greatest Common Divider
GND	Ground
HBM	Human Body Model
Hi-Z	High Impedance
I/O	Input / Output
ISO	International Standardization Organization
LC	Inductor-Capacitor
LCO	LC Oscillator
LSB	Least Significant Bit
MISO	Master-In Slave-Out
MOSI	Master-Out Slave-In

Term	Description
PA	Primary angle
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PGI	Programming Interface
POR	Power-On Reset
PTC	Programming-Through-Connector : Melexis programming tool via PGI
PWM	Pulse width modulation
RCO	RC Oscillator
rpm	Rotation per minute
Rx	Receiver
SA	Secondary angle
SAD	Set Circuit Address
SEooC	Safety Element Out-of-Context
SM	Serial Message
SPI	Serial Peripheral Interface
TDMA	Time Division Multiple Access
TSSOP	Thin-Shrink Small-Outline Package
T_A	Ambient temperature
Tx	Transmitter
VA	Vernier angle
VDP	Vernier divider primary
VDS	Vernier divider secondary
VM	Vernier multiplier
VP	Peak voltage
VPP	Peak to peak voltage
$V_{SE,pp}$	Single-ended peak to peak voltage

Table 2: Glossary of terms

3 Marking, pin definitions and descriptions

For more information see application diagrams in Section 12.

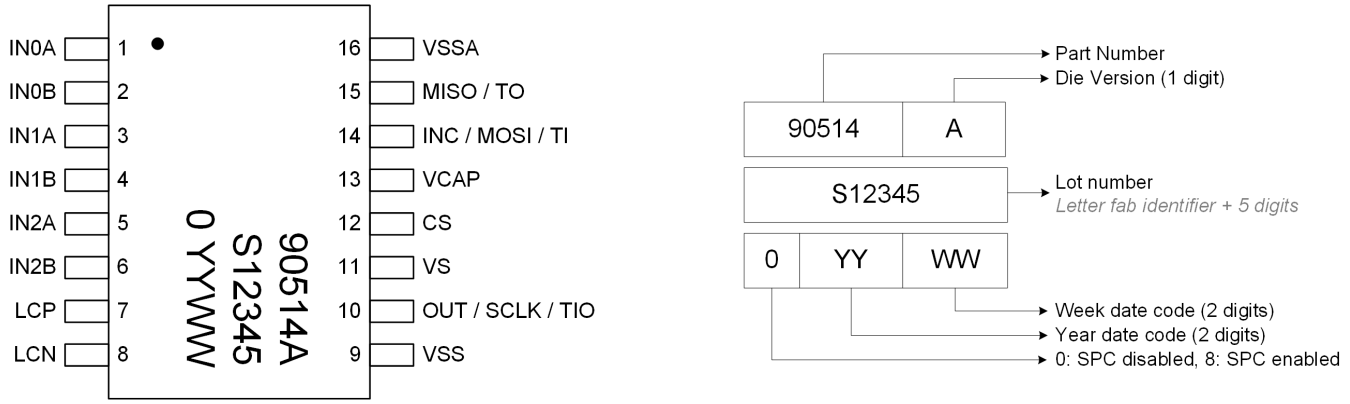


Figure 2: TSSOP-16 pin names and marking

Pin	Name	I/O type	Description
1	IN0A	I	Sensor receiver coil signal input 0, channel A
2	IN0B	I	Sensor receiver coil signal input 0, channel B
3	IN1A	I	Sensor receiver coil signal input 1, channel A
4	IN1B	I	Sensor receiver coil signal input 1, channel B
5	IN2A	I	Sensor receiver coil signal input 2, channel A
6	IN2B	I	Sensor receiver coil signal input 2, channel B
7	LCP	O	Transmitter coil, positive connection
8	LCN	O	Transmitter coil, negative connection
9	VSS	Ground	Digital, LCO and output driver ground
10	OUT / SCLK / TIO	I/O	SENT, PWM or SPC output / SPI serial clock input / PGI half-duplex input/output
11	VS	Power	Power supply voltage
12	CS / TCK	I	SPI - CS (chip select) / Test clock
13	VCAP	Power	External supply buffer capacitor connection
14	INC / MOSI / TI	I	PWM input C / SPI - MOSI / Test input
15	MISO / TO	O	SPI - MISO / Test output
16	VSSA	Ground	Analog ground

Table 3: TSSOP-16 pin definition and description

4 Absolute Maximum Ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Ambient temperature	T_A	-40		160	°C	
Junction temperature	T_{JUNC}			175	°C	
Storage temperature	$T_{STORAGE}$	-55		175	°C	
Supply voltage	VS	-18		18	V	Continuous
	VS	-24		24	V	t < 1 h
ESD CDM robustness	V_{CDM}			±500	V	All pins, according to AEC-Q100-011
	V_{CDM}			±750	V	Package corner pins
ESD HBM robustness	V_{HBM}			±4	kV	According AEC-Q100-002, for global pins VS, VSSA, VSS, OUT
	V_{HBM}			±2	kV	According AEC-Q100-002, for local pins INx, LCP, LCN, VCAP, INC, CS, MISO
Output overvoltage	V_{OUT}	-18		18	V	Continuous
Pin voltage range INx	V_{INx}	-0.3		5.5	V	
Pin voltage range LCP, LCN	V_{LCN}/V_{LCP}	-2.0		5.5	V	
Pin voltage range INC, CS, MISO	$V_{INC}/V_{CS}/V_{MISO}$	-0.3		5.5	V	
Pin voltage range VSSA, VSS	VSSA/VSS	-0.3		0.3	V	

Table 4: Absolute maximum ratings

5 General electrical specifications

MLX90514 Electrical Specifications are given in Table 5.

T_A = -40 °C to 160 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Position signal accuracy [1]	$Acc_{position}$	-0.36		0.36	°el	Applies to φ_{DLCA}, φ_{DLCB}
Position signal rms noise [2]			0.025		°el	LFC = 0, 1, 2
			0.035		°el	LFC = 3, 4
			0.055		°el	LFC = 5
Passive Diagnostic Output Level (Broken-Wire Detection)	BVSPD		0.0	0.5	%VS	Broken VS, R_{PD} < 10 kΩ
Passive Diagnostic Output Level (Broken-Wire Detection)	BVSPU	95.0	98.0		%VS	Broken VS, R_{PU} < 10 kΩ
Passive Diagnostic Output Level (Broken-Wire Detection)	BVSSPD		1.0	3.0	%VS	Broken GND, R_{PD} < 10 kΩ
Passive Diagnostic Output Level (Broken-Wire Detection)	BVSSPU	99.5	100.0		%VS	Broken GND, R_{PU} < 10 kΩ
Current limitation on pin OUT during short circuits	I_{OUTSC}	-16		-8	mA	Short to voltages > VS
	I_{OUTSC}	8		16	mA	Short to voltages < GND
Supply current operation	I_{VS}			12	mA	LCO disabled, No OUT load
	I_{VS}			20	mA	LCO: Q = 18
Inrush current	$I_{VS\_startup}$		50	100	mA	C_{VS} = C_{VCAP} = 470 nF, VS rise time > 100us
Digital Open Drain Output Leakage	I_{leak_od}			300	µA	R_{PU} at external voltage V_{EXT} < 18 V
	I_{leak_od}	-9		9	µA	V_{OUT} = 90 % VS in OD_{NMOS}, V_{OUT} = 10 % VS in OD_{PMOS}
Hi-Z Mode Output Leakage	I_{leak_HiZ}	-25		25	µA	$0 \leq V_{OUT} \leq VS$
Digital Output ON Resistance High Side	R_{ON_HS}	45		150	Ω	
Digital Output ON Resistance Low Side	R_{ON_LS}	27		130	Ω	
SENT Output Resistance	R_{OUT_SENT}	100		205	Ω	

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Thermal resistance - junction to ambient	R_{thja}			99	K/W	
Thermal resistance - junction to case	R_{thjc}			27	K/W	
Supply Voltage	VS	4.5	5.0	5.5	V	
VS POR voltage IC OFF	VPORB_HL	1.50	1.85	2.00	V	
VS POR voltage IC ON	VPORB_LH	2.05	2.45	2.70	V	
SENT Output Dynamic Level high	V_{SENT_hi}	4.15		4.6	V	Pulse shaping mode, 10 kΩ > R_{PU} > 55 kΩ
SENT Output Dynamic Level low	V_{SENT_lo}	0.05		0.3	V	Pulse shaping mode, 10 kΩ > R_{PU} > 55 kΩ
EEPROM programming temperature	T_{EEPROM}	-40		125	°C	
EEPROM erase/write cycles				600		per row and column

Table 5: Electrical and system level performance specification

[1] The value reported is a ±3σ value including noise assuming LFC = 0 settings, but does not include latency contributions and contributions from the output physical layer, the latter being relevant for the PWM output mode. The value reported is valid within the speed and acceleration ranges detailed in Section 7.4.1, and with ideal, offset free input signals. For errors related to the input signal offset compensation, refer to Section 7.5.1.

[2] The value refers to room temperature with minimum signal strength. Higher signal strength reduces the noise. Lower noise can also be achieved with disabled acceleration compensation (DSP_ACC_DIS = 1).

6 Timing specification

6.1 General timing Specifications

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 160 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LCO start-up time	$T_{startup\_LCO}$		20	100	µs	
RC oscillator frequency	f_{RCO}	19.3	20	20.7	MHz	Factory trimmed
Application clock	f_{AC}	$f_{RCO}/4$		f_{RCO}	MHz	
Latency	$\Delta\tau_{phi}$	1 -1		3 0	µs	ABE_AOUT_MODE = 1,2,3 ABE_AOUT_MODE = 4,5
Initialization time [1]	T_{INIT}	0.5	0.7	0.9	ms	f_{AC} = 20 MHz
Start-up time [1]	T_{STUP}	0.7 2.8 11.1	1.0 2.9 11.2	2 [2] 3.0 11.5	ms ms ms	MUPET_CAP = 3 MUPET_CAP = 1 MUPET_CAP = 0

Table 6: General timing parameters

[1] VS rise time from 0 V to 5 V in 100 µs,

[2] DSP_LFC_HI $\geq$ 5, f_{AC} = 20 MHz

The application clock frequency f_{AC} is controllable by field AC_SEL [2:0] with following mapping:

AC_SEL	f_{AC} [MHz] (typ.)
3	10
5	5
0 (default)	20

Table 7: Application clock frequency f_{AC} programming

A lower application clock reduces the MLX90514 current consumption for digital signal processing and ADC but comes with restrictions on dynamic characteristics and communication speed, e.g. SENT tick times (refer to Table 25).

6.2 Startup time

The startup time T_{STUP}, see Table 6 is the duration between power-on reset (POR) until the output interfaces are enabled and the internal angular acquisition has finished.

With enabled cold activation of the MUPET programming interface (MUPET_CAP $\neq$ 3) pin OUT stays in Hi-Z until T_{STUP} independent from acquisition procedure of the angular data, see Table 6. This in turn delays all

communication on PWM, SENT/SPC and SPI accordingly. No SPC trigger pulse and no SPI clock should be applied before T_{STUP}. For SENT and PWM the frame transmission starts after T_{STUP}.

Without MUPET cold activation (MUPET_CAP = 3) T_{STUP} is the sum of T_{INIT} and a period for the DSP angular acquisition. While the output interfaces are enabled after T_{INIT} they report safe state until the DSP confirms valid angular data.

For all communication interfaces during startup the sensor reports safe state SS2 (Hi-Z) or SS3, see Section 10.3.

In SENT/SPC mode the first transmitted frame will be marked as initialization frame with FC1 set to zero, refer to Figure 3. With MUPET_CAP = 3 the interface is enabled after T_{INIT} and all frames until T_{STUP} are set to invalid as well.

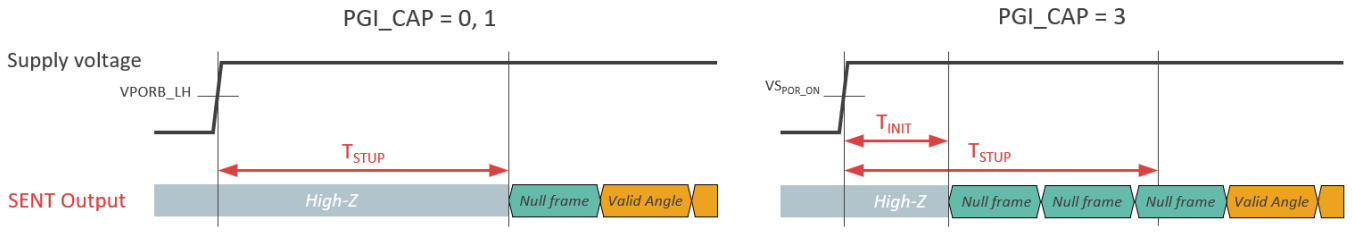


Figure 3: IC startup in SENT mode

In PWM mode the first transmitted frame will be have a duty cycle of zero.

7 Detailed description

7.1 Block diagram

The MLX90514 is an inductive position sensor which is used for absolute rotary or linear motion/position sensing (defined by the coil system). In Figure 4 the block diagram is given.

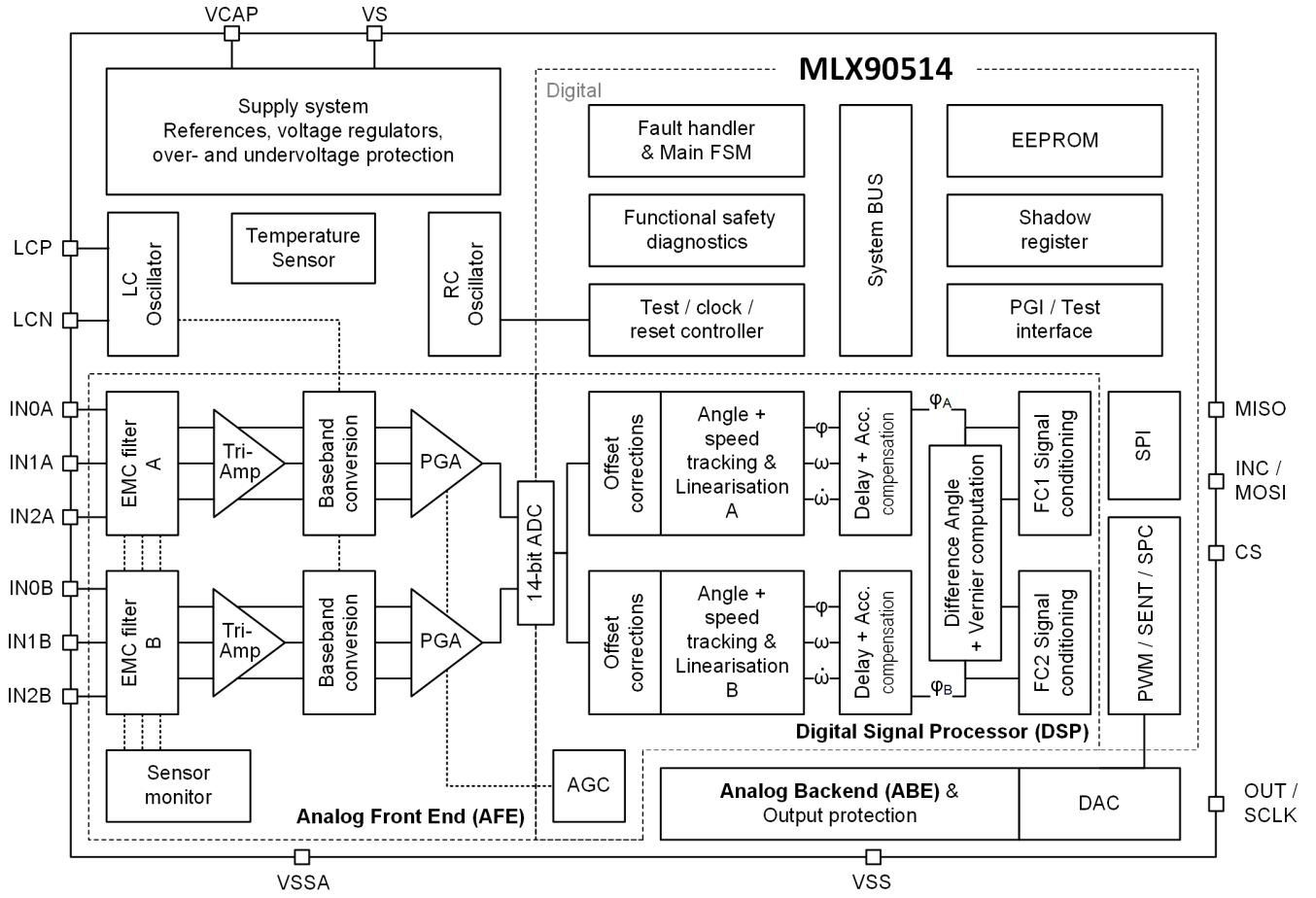


Figure 4: Block diagram

The main functional sections are: sensor excitation with an LC Oscillator (LCO), the Analog Front-end (AFE) performing the sensor position signal analog pre-processing, the Analog-To-Digital Conversion (ADC) followed by the Digital Signal Processing (DSP) and an Analog Back-end (ABE) providing the output signal.

The AFE consists of two channels A and B, each equipped with an EMC filter, Tri-Amplifier, baseband conversion and a Programmable Gain Amplifier (PGA). A third input INC allows to receive and process external sensor data with PWM. The digital core provides the signal processing for angular computation and system control as well as the protocol engines for SENT, SPC and PWM. The ABE consists of a highly flexible output driver with output protection against overvoltage and overcurrent. The main supporting functionalities are the supply system, functional safety diagnostics, the customer programming interface (PGI), the Serial Peripheral Interface (SPI) and an EEPROM for the system configuration data storage.

The functional safety concept provides self-diagnostic features to check the integrity of the sensor coil system, the integrity of the input and output signals, and the IC itself.

7.2 Supply system

The MLX90514 has an integrated supply system providing regulated supply and reference voltages, as well as bias currents.

These regulated supply voltages guarantee immunity against disturbances on the external power supply, required for the correct functionality of the sensor IC. The capacitance at the pin VCAP, refer to Section 12, serves as an energy storage during short VS voltage dips.

The supply system offers safety mechanisms and monitors for over- and undervoltage protection, reverse-polarity protection and power control to ensure correct sensor operation.

7.3 Sensor coil system

MLX90514 is designed for an external sensor (coil system) consisting of one transmitting coil (Tx) and two sets of three receiving (Rx) coils each. The parameters described in this section specify the electrical characteristics of the sensor coil system, but do not constitute a full inductive sensor design guideline. For details and support for the sensor and target design please contact the Melexis sales office.

7.3.1 Tx coil and LC Oscillator

The LCO drives the Tx coil of the sensor coil system. The LCO frequency (f_{LCO}) is defined by the external inductance (L_{Tx}) and the two external capacitors C_{LCO} (see Figure 5). A customization of the frequency is possible by variation of L_{TX} and C_{LCO}. The R_{TX} represents the internal resistance of the Tx coil.

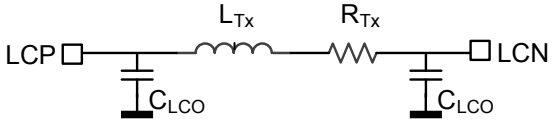


Figure 5: LCO Tx coil model

The LCO frequency can be calculated using the flowing formula:

$$f_{LCO} = \frac{1}{2\pi}\sqrt{\frac{1}{L_{Tx}\cdot(C_{LCO}/2)} - \left(\frac{R_{Tx}}{L_{Tx}}\right)^2}$$

The LCO amplitude can be scaled by setting LC_OSC_AMP to 1. A reduced LCO amplitude is used for cases where the maximum input signal amplitude (A_{Rotor}) is exceeded (refer to Section 7.4.1) or to reduce emissions.

The LCO frequency (f_{LCO}) is defined by the Tx coil inductance (L_{Tx}) and the external capacitors (C_{LCO}). A customization of the frequency is possible by variation of L_{Tx} and C_{LCO}. As an example, for a typical value of f_{LCO} = 2.7 MHz, the external components can be set as L_{Tx} = 4 µH and C_{LCO} = 1.8 nF. However, other component value combinations within the specification range are applicable.

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 160 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
LCO frequency range	f_{LCO}	2.0	2.7	5.0	MHz	
LCO common mode voltage	V_{CM}		1.68		V	
LCO amplitude	A_{LCO}	2.05	2.4	2.7	$V_{SE,pp}$	LC_OSC_AMP = 0
Scaled LCO amplitude	A_{LCO}	1	1.4	1.55	$V_{SE,pp}$	LC_OSC_AMP = 1
Tx coil inductance	L_{Tx}	1	4[2]	10	µH	
Tx coil internal resistance	R_{Tx}		5[2]		Ω	
Capacitor	C_{LCO}		1.8		nF	
Tx quality factor	Q_{Tx}		18[1,2]			
LCO current consumption	I_{VS_LCO}		3[2]		mA	

Table 8: LCO electrical parameters

[1] Tx Quality factor can be calculated with $Q_{TX} = 2\pi \cdot f_{LCO} \cdot L_{Tx} / R_{Tx}$

[2] See Figure 6 for relation between Q_{Tx} and I_{VS_LCO} (typical conditions)

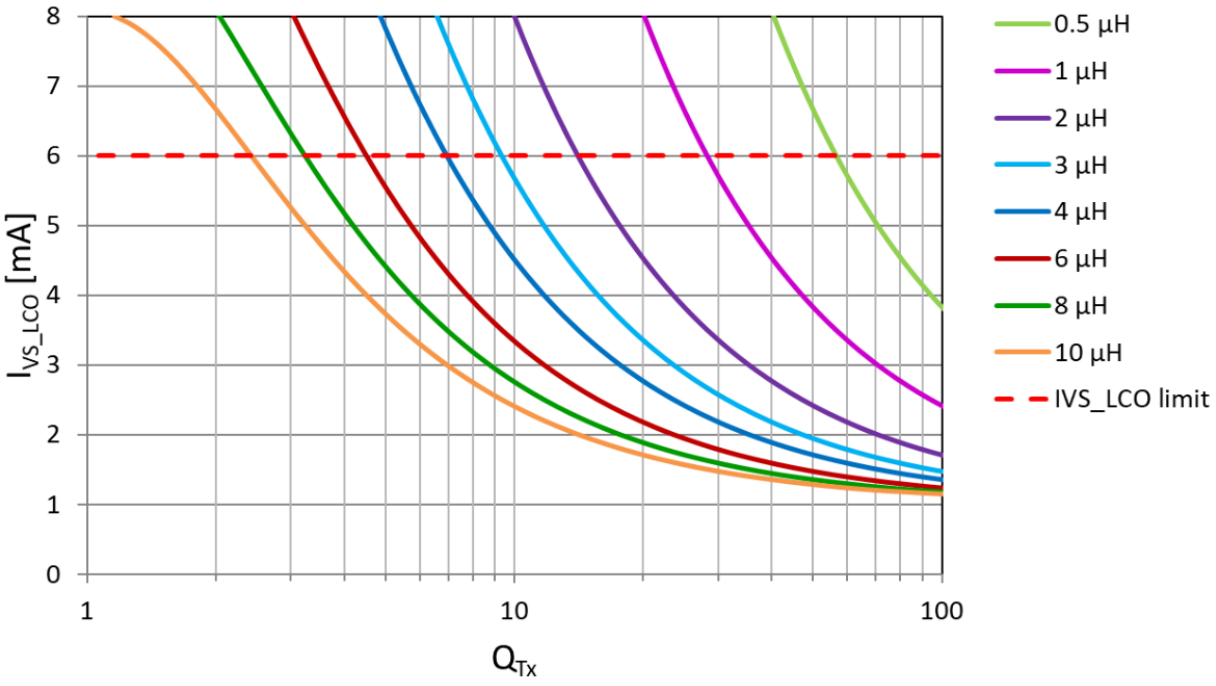


Figure 6: I_{VS_LCO} as function of Q_{TX} for f_{LCO} = 2.7 MHz

7.3.2 Rx Coils

The Rx coils electrical specification is given in Table 9. For details and support regarding sensor coil system designs please contact the Melexis sales office.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Rx Inductive component	L_{Rx}	40	200	500	nH	

Table 9: Rx coils specification

Each individual Rx coils set is DC biased by the internal Sensor Bias circuits. Three individual DC operating points per Rx coil set can be chosen by EEPROM register CIDA and CIDB programming for channel A and B, respectively.

For a single sensor module, the default Sensor Bias setting can be used. For a multi-sensor module including more than two sensor coil systems, the DC operating point of the individual sensors must be programmed to different values (CIDA and CIDB setting) for the correct safety function of the sensor short detection.

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 160 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Sensor Bias operating point	V_{SOP}	0.66	0.7	0.74	V	CIDA / CIDB = 0 (CIDA default value)
		0.99	1.04	1.09		CIDA / CIDB = 1 (CIDB default value)
		1.35	1.41	1.47		CIDA / CIDB = 2, 3

Table 10: Sensor DC operating points

7.4 Analog signal processing

The transmit coil, excited by the LCO, inductively couples to the two sets of Rx coils corresponding to the A and B channels. The coils are connected to the pins IN0A, IN1A, IN2A and IN0B, IN1B, IN2B, respectively. The strength of the coupling is modulated by the rotor position and leads to amplitude modulated receive signals at LCO frequency.

7.4.1 Input signal specification

The three input signal envelopes from each of the sensor coil sets INxA and INxB are composed of an angular signal of amplitude A_{RotorA} and A_{RotorB}, the common mode level $A_{CommonA}$ and $A_{CommonB}$, and the asymmetry A_{AsymxA} and A_{AsymxB} respectively, according to the formulas below.

$$IN0A,B = A_{RotorA,B} \sin\left(\phi_{A,B} - \frac{1}{6}\pi\right) + A_{CommonA,B} + A_{Asym0A,B}$$
$$IN1A,B = A_{RotorA,B} \sin\left(\phi_{A,B} - \frac{5}{6}\pi\right) + A_{CommonA,B} + A_{Asym1A,B}$$
$$IN2A,B = A_{RotorA,B} \sin\left(\phi_{A,B} - \frac{9}{6}\pi\right) + A_{CommonA,B} + A_{Asym2A,B}$$

$A_{CommonA,B}$ is caused by a common mode direct coupling from the Tx coil into the Rx coils and is equal on all three inputs. The common mode voltage is suppressed by the MLX90514.

$A_{AsymxA,B}$ is caused by the asymmetry of the Rx coils on the PCB. It can have different offset voltages on each INx signal caused by feeding lines from and to the sensor PCB or metal objects close to the PCB sensor. This coil system asymmetry level causes a first-order harmonic on the measured angle and should be compensated using the MLX90514 DC-compensation methods (refer to Section 7.5.1).

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 160 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit
INx input signal envelope	A_{RotorA} A_{RotorB}	2.5		100	mV_P
INx common mode amplitude	$A_{CommonA}$ $A_{CommonB}$			min(700 mV, 10 · A_{RotorA}) min(700 mV, 10 · A_{RotorB})	V
INx asymmetry amplitude	A_{AsymA}[1] A_{AsymB}[2]			min(10 mV, 0.7 · A_{RotorA}) min(10 mV, 0.7 · A_{RotorB})	V

Table 11: Input signal requirements

[1] $A_{AsymA} = max(|Asym0A|, |Asym1A|, |Asym2A|)$

[2] $A_{AsymB} = max(|Asym0B|, |Asym1B|, |Asym2B|)$

The maximum input signals frequency (angular speed) is given in Table 12.

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 160 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Electrical angular speed	v_{el}	-240 000[1]		240 000[1]	e-rpm	f_{AC} = 20 MHz

Table 12: Electrical rotational speed

[1] If f_{AC} < 20 MHz, this value should be rescaled by a factor f_{AC} [MHz] / 20. It is recommended to consider as well the Nyquist criteria

The maximum input signals frequency variation (angular acceleration) depends on the bandwidth of the phase tracking loop (refer to Section 7.5.2), which is controlled by the LFC parameter as listed in Table 13. The LFC parameter is automatically adapted by the system on the basis of the measured acceleration. The user can restrict the LFC lower and upper bounds via the fields DSP_LFC_LO [2:0] and DSP_LFC_HI [2:0], respectively. Note that Table 13 refers to an application clock f_{AC} = 20 MHz. For other values, the acceleration limits should be scaled by a factor $(f_{AC}$ [MHz]/20)^2.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Electrical angular acceleration	a_{el}	-18 750		18 750	e-rpm/s	LFC = 0
		-75 000		75 000		LFC = 1
		-300 000		300 000		LFC = 2
		-1 200 000		1 200 000		LFC = 3
		-4 800 000		4 800 000		LFC = 4
		-19 200 000		19 200 000		LFC = 5

Table 13: Electrical rotation acceleration with f_{AC} = 20 MHz, DSP_SROS = 2

7.4.2 Filtering, amplification and rectification

The input signals INxA and INxB are filtered through the EMC filter to suppress high frequency noise. The common mode of the input signals voltage, caused by symmetrical coupling from the Tx coil, is suppressed by a differential amplifier stage.

The rectifier and low pass filter blocks perform a rectification of the amplifier output signals. The rectification is based on the clock derived from the LCO.

7.4.3 Automatic Gain Control

The rectified signals are subject to an amplification step before being converted to digital signals by the ADC block. The MLX90514 has an automatic gain control (AGC) with 5 gain settings operating independently on channel A and B. The fields AGC_GAIN_MIN [2:0] and AGC_GAIN_MAX [2:0] allow to restrict the AGC dynamic range or even to lock it by programming AGC_GAIN_MIN = AGC_GAIN_MAX. Restricting the AGC range is not recommended and may result in a reduced range for A_{Rotor} as shown in Figure 7, however the self-monitoring of the AGC operation is not affected. The currently selected AGC gain is reported with registers AGC_GAIN_A and AGC_GAIN_B respectively.

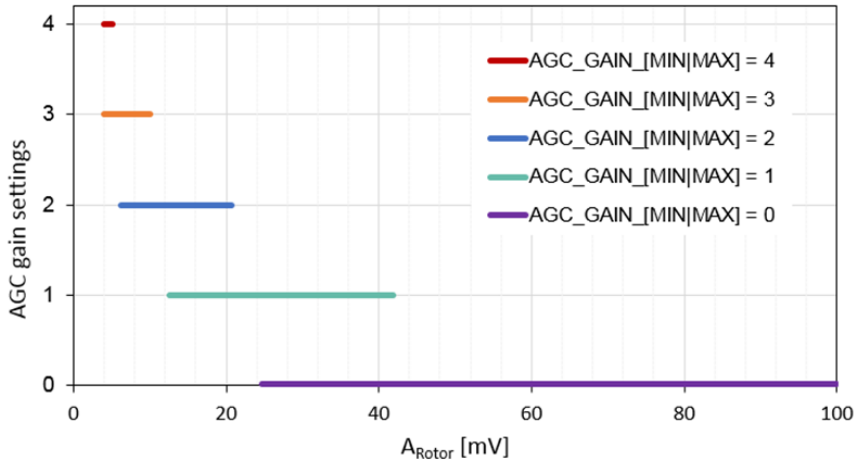


Figure 7: AGC gain settings as a function of A_{Rotor}

7.5 Digital Signal Processing (DSP)

The ADC permanently provides sequential samples to the DSP, including samples of the six INx input phase differences, LCO amplitude samples and functional safety test measures.

The DSP features two parallel tracks, one for channel A and one for channel B, each comprising a DC offset compensation, interpolation (to align all three phases to a common sampling point), conversion from 3-phase to I/Q domain, a tracking phase-locked loop and a linearization option. The output angles are compensated regarding processing delay utilizing estimated speed and acceleration, resulting in the two angles φ_{DLCA} and φ_{DLCB}. The MLX90514 can also read in a PWM signal on pin INC making available a third angle φ_C.

The DSP features a difference angle, a mean angle, and a Vernier angle calculation unit which can work on any pair of the φ_{DLCA}, φ_{DLCB} and φ_C angles. Two signal conditioning units complement the DSP.

7.5.1 Digital offset compensation methods

In Section 7.4.1 the composition of the INx signals is given. The signals $A_{Asym0A,B}$, $A_{Asym1A,B}$ and $A_{Asym2A,B}$ are DC offsets of the input signals of the A (INxA) and B (INxB) channels, respectively, being mainly caused by asymmetries of the PCB coil design (Rx and Tx coils), and caused by feeding lines from and to the sensor or metal objects close to the sensor. This asymmetry can be compensated in the MLX90514 by setting the fields DC01A [15:0], DC12A [15:0] and DC20A [15:0] for channel A, and DC01B [15:0], DC12B [15:0] and DC20B [15:0] for channel B. The compensation methods are fully automated in the PTC-04/PTC-05 programming tool. To ensure ASIL-C compliance and accuracy, it is mandatory to perform DC offset compensation.

The offset compensation is subject to thermal drifts whose magnitude is dependent on the LCO frequency and the ratio between the amount of compensated A_{Asym} and the useful signal strength A_{Rotor}. The thermal drift dependence on these two parameters is illustrated in Figure 8 assuming that the offset compensation is performed at 35 °C.

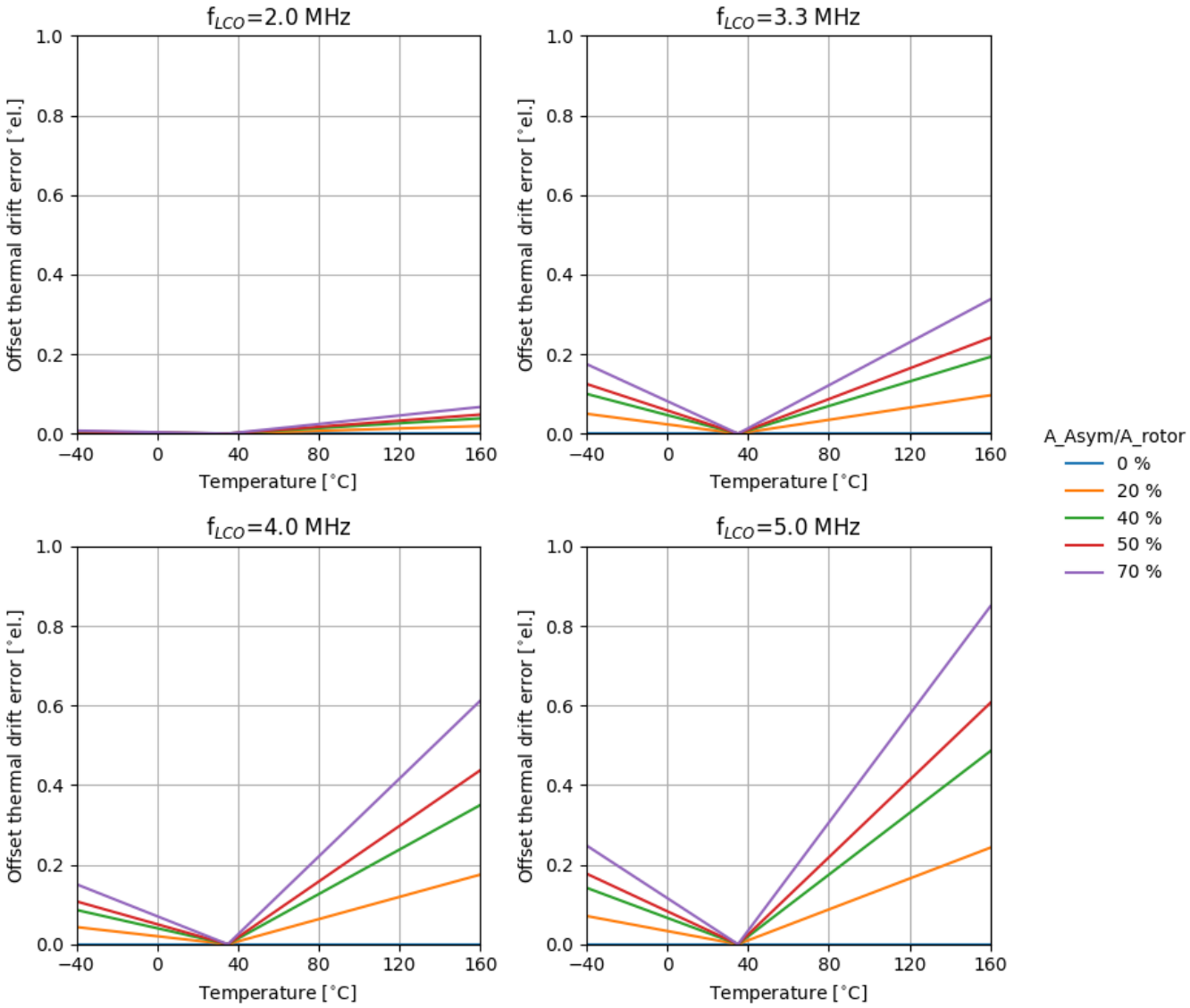


Figure 8: Offset thermal drift error

7.5.2 Phase tracking loop

The phase tracking loop calculates the angle, speed and acceleration of the input signals envelope per channel A and B. The phase tracking loop is characterized by a finite bandwidth that limits the maximum acceleration allowed for the input signals. The band-width (see of the tracking loop Figure 9) is determined by the loop filter coefficient (LFC), controllable via fields DSP_LFC_LO [2:0] and DSP_LFC_HI [2:0] , refer to Section 7.4.1.

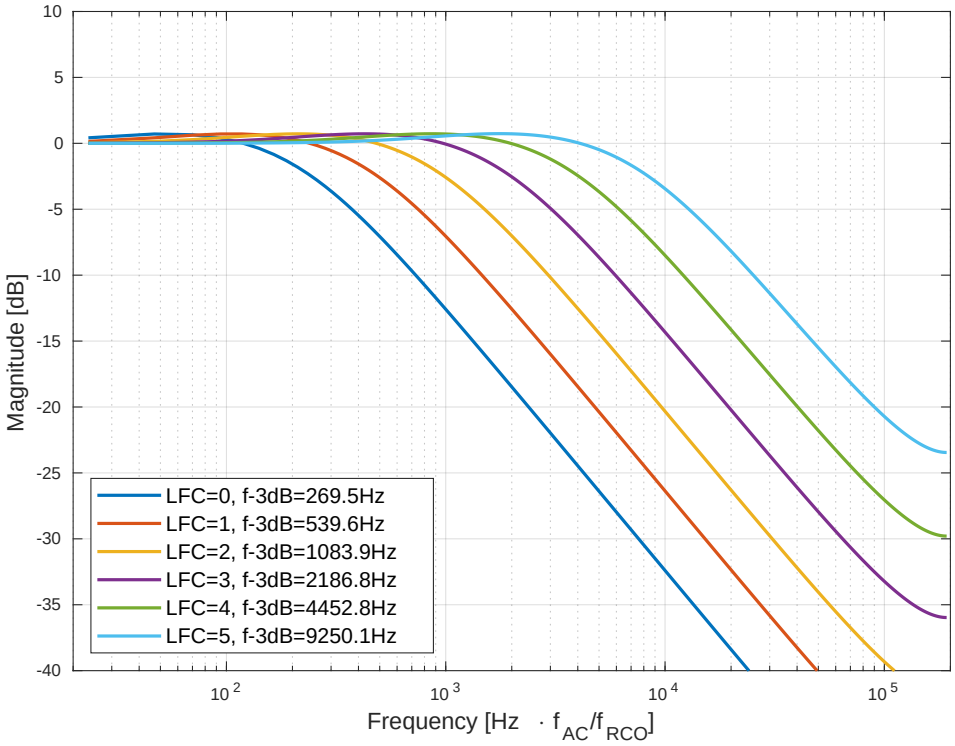


Figure 9: Phase tracking loop frequency response

The 16-bit 2's-complement angle estimates including linearization (refer to 7.5.3) reflect the electrical angle per channel as:

$$\varphi_{A/B}[^\circ el] = LIN\_PHASE_{A/B}/2^{16} \cdot 360^\circ el$$

The 17-bit 2's-complement speed estimates (range [-(2^{16}),2^{16}-1]) reflect the electrical rotational speed as:

$$v_{elA/B}[e\text{-}rpm] = \frac{SPEED\_HI_{A/B} \cdot 2^{16} + SPEED\_LO_{A/B}}{2^{23}} \cdot \frac{f_{AC} \cdot 60}{26}$$

Table 14 depicts the expected range of the electrical speed estimate depending on the application clock and whether the 16-bit or 17-bit SPEED value is evaluated.

f_{AC} [MHz]	{SPEED_HI, SPEED_LO} max(|v_{el}|) [e-rpm]	SPEED_LO max(|v_{el}|) [e-rpm]
20	350000	175000
10	175000	87500
5	87500	43750

Table 14: Electrical speed depending on f_{AC} and width of SPEED value

The RCO frequency tolerance limits the absolute accuracy of the rotational SPEED estimate. A calibration is possible by measuring the PWM frequency in PWM mode or via synchronous interfaces (SPI) reading the PWM

period counter value PWM_PCNT [15:0], which runs continuously in range [0, T_FRAME-1] with time resolution $1/f_{AC}$. In non-PWM output modes PWM_PCNT needs to be enabled with PWM_PCNT_ON set to 1.

7.5.3 16-Point linearization

The 16-point linearization allows to equalize angular non-linearity errors which can be caused by asymmetries in the sensor coil system layout. Being a sub-block of the phase tracking DSP, the equalization works speed independent. Both the A and B channels dispose of dedicated linearization functions.

The 16 equalization values LINA00 [7:0] to LINA15 [7:0] (2's-complement, range [-(2^7),2^7-1]) characterize the angular error curve at angular sample points $[0 \ldots 15]/16 \cdot 360$ [°el] which is applied to the channel A angle. The values LINB00 [7:0] to LINB15 [7:0] apply for channel B likewise. All intermediate values are linearly interpolated, see Figure 10. After equalization, the residual error curve is the difference between the input error curve and the interpolated equalization curve. The characterization of the equalization coefficients LINAxy and LINBxy should be performed in quasi-static or low-speed application mode. With increasing rotational speed, the 16-point linearization automatically adapts to the low pass band limitation of the error curve.

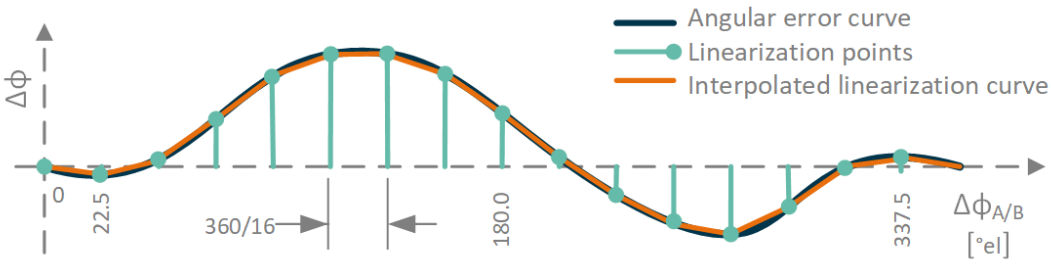


Figure 10: Angular error curve compensation

Depending on LINA_GAIN [2:0] and LINB_GAIN [2:0], the gain of the equalization curve can be adjusted for the A and B channels, respectively. If LIN[A,B]_GAIN is set to 0, no equalization is applied. For LIN[A,B]_GAIN = [1 ... 7] the error curve is adjusted per sample point as:

$$\Delta\varphi = signed\,(LIN[A,B]xy) \cdot 2^{LIN[A,B]\_GAIN-17} \cdot 360\,[^{\circ}el]$$

The signed 8-bit equalization values LIN[A,B]00 to LIN[A,B]15 have a range of [-127:127] each. Table 15 indicates the equalization range versus resolution per sample point.

LIN[A,B]_GAIN [2:0]	Resolution [deg]	Range (±) [deg]
0	0	0
1	0.0055	0.70
2	0.011	1.40
3	0.022	2.79
4	0.044	5.58
5	0.088	11.16

LIN[A,B]_GAIN [2:0]	Resolution [deg]	Range (±) [deg]
6	0.176	22.32
7	0.352	44.65

Table 15: Linearization range

The calculated angle after linearization and before delay compensation and zero position adjustment can be monitored via the register LIN_PHASE_A [15:0] and LIN_PHASE_B [15:0] (refer to Section 11.3).

The linearization is part of the phase tracking loop (refer to Section 7.5.2) making the angular equalization independent from rotational speed. During calibration of the equalization values it is advised to perform it at low rotational speed or configure the phase tracking loop filter to high bandwidth, (see Figure 9).

7.5.4 Delay compensation and zero position adjustment

The speed signal provided by the phase tracking loop (refer to Section 7.5.2) is used to compensate for phase errors due to the system latency, while the acceleration signal is used to compensate for phase errors during acceleration due to the latency of the speed calculation. The user furthermore disposes of the programmable field DELAY_ANA to compensate for additional delays associated to e.g. filter networks in between the IC and the ECU, in steps of $3.25/f_{RCO}$.

As a final complement, the mechanical position of the target resulting in zero output value for channels A and B can be adjusted by setting the fields PHASE_OFS_A[15:0] and PHASE_OFS_B[15:0], respectively. The values of these fields are systematically added to the position values calculated by the phase tracking loops.

The two calculated angles after delay compensation and zero position adjustment can be monitored via the register SC_FC1 [15:0] and SC_FC2 [15:0] (refer to Section 7.5.9), hereafter referred to as φ_{DLCA} and φ_{DLCB}.

7.5.5 External PWM input

By setting the field PWMRX = 1, the MLX90514 receives a pulse width modulation from pin INC and calculates a 16 bits 2s-complement value φ_C [15:0] representing an 0...360 °el angle with resolution 360 °el/2^{16}. The receiver measures the period of the received PWM C_{PWM} and the duty cycle duration C_{DC} relative to the application clock f_{AC} and computes the PWM duty cycle as:

$$DC = 2^{16}\frac{C_{DC}}{C_{PWM}}$$

The computed DC value is converted to φ_C according to the fields PWMRX_X1 [15:0] and PWMRX_X2 [15:0] as follows:

$$\varphi_c[15:0] = \begin{cases} DC\,[15:0] & \text{, if PWMRX\_X1 = PWMRX\_X2 = 0} \\ \frac{DC-\text{PWMRX\_X1}}{\text{PWMRX\_X2}-\text{PWMRX\_X1}} \cdot (2^{16}-1) & \text{, else} \end{cases}$$

The polarity of the PWM pulse can be adjusted by the field PWMRX_INV. If PWMRX_INV = 0, the low-state duration is proportional to the transmitted data. If PWMRX_INV = 1, the high-state duration is proportional to the transmitted data.

Similar to the A and B channels, the 0 position of the φ_C angle can be controlled via the PHASE_OFS_C [15:0] field, which is systematically added to φ_C.

If PWMRX = 0, then φ_C [15:0] = 0. Note that the INC function is not available in conjunction with SPI sharing the MOSI pin.

7.5.6 Difference angle calculation

The MLX90514 calculates the difference between a pair of angles φ_{MIN} and φ_{SUB} selectable by the DIFF_CFG [2:0] field among φ_{DLCA}, φ_{DLCB} and φ_C according to Table 16.

DIFF_CFG [2:0]	φ_{MIN}	φ_{SUB}
0	φ_{DLCA}	φ_{DLCB}
1	φ_{DLCA}	φ_C
2, 3	φ_{DLCB}	φ_C
4	φ_{DLCB}	φ_{DLCA}
5	φ_C	φ_{DLCA}
6, 7	φ_C	φ_{DLCB}

Table 16: ϕ_{MIN} and ϕ_{SUB}

Note, that the inputs φ_{MIN} and φ_{SUB} must have the same rotation direction.

The difference angle φ_{DIFF} [15:0] is calculated according to the formula:

$$\varphi_{DIFF} = mod\left(N_{SUB} \cdot \varphi_{MIN} - N_{MIN} \cdot \varphi_{SUB},\ 2^{16}\right)$$

Where N_{MIN} and N_{SUB} are defined by the fields DIFF_N_MIN [5:0] and DIFF_N_SUB [5:0], respectively, and correspond to the number of electrical periods per mechanical period of φ_{MIN} and φ_{SUB}, divided by their greatest common divider GCD. In other words, φ_{MIN} accomplishes $N_{MIN} \cdot$ GCD electrical periods per mechanical period, while φ_{SUB} accomplishes $N_{SUB} \cdot$ GCD electrical periods per mechanical period.

φ_{DIFF} represents a mechanical angle difference expressed with 16 bits resolution. The relation between the mechanical angle expressed in degrees φ_{DIFF} [°mech] and φ_{DIFF} [15:0] is as follows:

$$\varphi_{DIFF}[^\circ mech.] = \frac{\varphi_{DIFF}[15:0]}{GCD \cdot N_{MIN} \cdot N_{SUB}} \cdot \frac{360}{2^{16}}$$

with the range for φ_{DIFF} [°mech] being:

$$\frac{-180}{GCD \cdot N_{MIN} \cdot N_{SUB}} < \varphi_{DIFF}[^{\circ}mech.] < \frac{180}{GCD \cdot N_{MIN} \cdot N_{SUB}}$$

7.5.7 Difference compensated angle calculation

Thanks to the difference angle being available, the MLX90514 can translate the φ_{MIN} angle to the periodicity of the φ_{SUB} angle and vice versa, depending of the configuration of the DIFF_CS field as per Table 17.

DIFF_CS	0	1
Formula	$\varphi_{CBD} = mod\left(\varphi_{SUB} + \frac{\varphi_{DIFF}}{N_{MIN}}, 2^{16}\right)$	$\varphi_{CBD} = mod\left(\varphi_{MIN} - \frac{\varphi_{DIFF}}{N_{SUB}}, 2^{16}\right)$
Description	φ_{CBD} represents the electrical angle φ_{MIN} with $GCD \cdot N_{SUB}$ electrical periods per mechanical period	φ_{CBD} represents the electrical angle φ_{SUB} and has $GCD \cdot N_{MIN}$ electrical periods per mechanical period

Table 17: Difference compensated angle

7.5.8 Vernier angle calculation

The MLX90514 allows performing a Vernier angle calculation in between a primary angle PA and a secondary angle SA selected by the VER_CFG [2:0] field according to Table 18. The Vernier angle can be used for absolute position sensing.

VER_CFG [2:0]	PA	SA	VER_CFG [2:0]	PA	SA
0	φ_{DLCA}	φ_{DCLB}	4	φ_{DCLA}	φ_{C}
1	φ_{DLCB}	φ_{DLCA}	5	φ_{C}	φ_{DLCA}
2	φ_{CBD}	φ_{C}	6	φ_{DLCB}	φ_{C}
3	φ_{C}	φ_{CBD}	7	φ_{C}	φ_{DLCB}

Table 18: Vernier inputs selection

Here φ_A, φ_B and φ_C denote the delay compensated 16-bit electrical angle values from sensor channel A, B and the received PWM channel C respectively. φ_{CBD} is the output of the Difference Compensated Angle calculation, see Section 7.5.7. Note that PA and SA need to have the same rotation direction for correct Vernier calculation.

The Vernier angle VA is calculated from PA and SA according to the following formula:

$$VA = mod\left(\frac{PA + 2^{16} \cdot mod\left(VM \cdot round\left(\frac{VDS \cdot PA - VDP \cdot SA}{2^{16}}\right), VDP\right)}{VDP}, 2^{16}\right)$$

Where VDP is the Vernier divider primary defined by the field VER_VDP [5:0], VDS is the Vernier divider secondary defined by the field VER_VDS [5:0] and VM is the Vernier multiplier defined by the field VER_VM [5:0]. VDP corresponds to the number of electrical periods of the PA angle over a Vernier angle range, while VDS corresponds to the number of electrical periods of the SA angle over a Vernier angle range.

For a correct VA result VM needs to be configured to satisfy the following conditions:

$$mod\left((VDP - VDS) \cdot VM, VDP\right) = 1$$
$$VM < max(VDP, VDS)$$

For high resolution it is recommended to choose $VDP > VDS$.

An illustrative case of Vernier calculation is depicted in Figure 11, where the primary angle PA has 5 periods and the secondary angle SA has 3 periods per mechanical rotation. The Vernier angle VA represents 1 mechanical rotation.

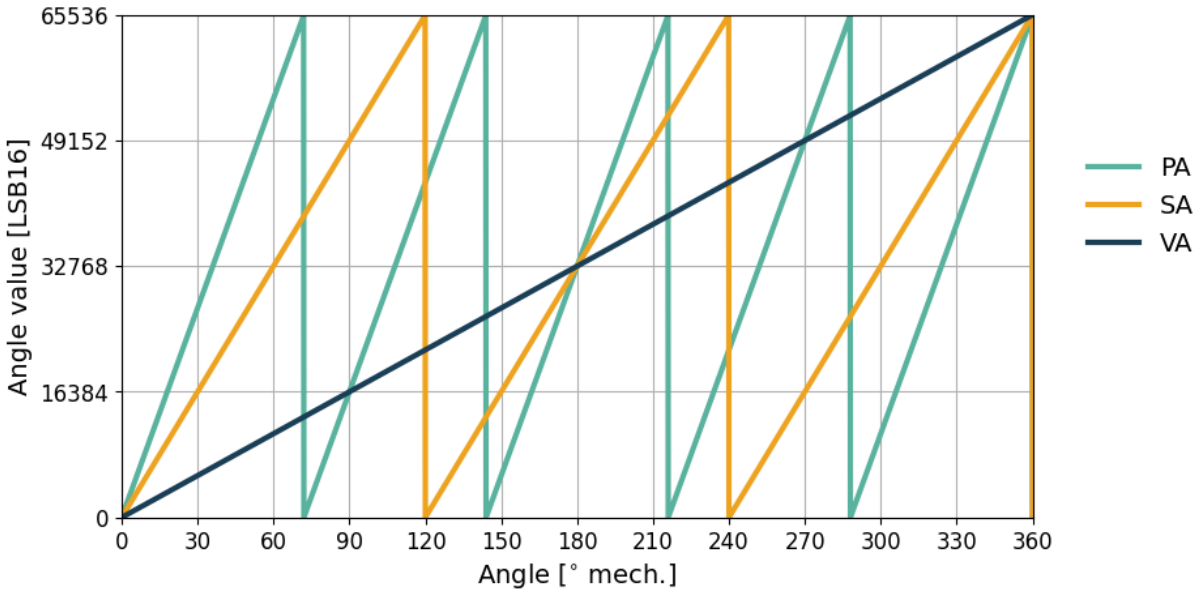


Figure 11: Example of Vernier calculation for VDP=5, VDS=3 and VM=3

The zero point of Vernier angle value depend on the zero point of the primary angle as:

$$VA_0 = \frac{PA_0}{VDP} \cdot \frac{2^{16}}{360}$$

For a robust calculation of the Vernier angle the primary and secondary angle should have the same mechanical zero position. Any offset between PA and SA can be determined by the Vernier reserve diagnostic DIAG_VRES, refer to 10.5.5. The 16-bit 2's-complement Vernier reserve value is computed as:

$$VRES = mod\left(mod\left(PA \cdot VDS + 2^{15}, 2^{16}\right) - mod\left(SA \cdot VDP, 2^{16}\right), 2^{16}\right) - 2^{15}$$

VRES near to +/-2^{15} will lead to selection of a wrong Vernier-section and corresponds to offsets of $\Delta SA\,[°\text{el}] = \pm 180\,°\text{el}/VDP$ or $\Delta PA\,[°\text{el}] = \pm 180\,°\text{el}/VDS$.

The Vernier calculation is executed with a sampling rate according to the PA input. If PA is φ_C, the VA is updated with the period of the PWM input modulation. If PA is not φ_C the VA is updated with the DSP sampling rate leading to an effectively continuous IC output value.

The VA accuracy depends only on PA as long as distortions or offsets on SA do no exceed the range $\pm 180\,°\text{el}/VDP$. If SA is φ_C the PWM input update period $1/f_{PWM}$ would create such an offset with increasing rotation speed due to the angular drift of the PA vs SA. In this case it is advised to limit the rotational speed as follows:

$$v_{mech}[rpm] < \frac{30 \cdot f_{PWM}}{VDP \cdot VDS}$$

7.5.9 Fast Channel mapping

The MLX90514 DSP supports two synchronous fast channel signal paths towards the output interfaces with independent signal conditioning according to the selected output mode. Any sensor path angle value or the computed results for difference or Vernier angle can be mapped onto these fast channels.

7.5.9.1 Fast Channel 1 (FC1)

The Fast Channel 1 (FC1) content can be selected by field FC1_CFG [2:0] per Table 19. The Fast Channel 1 can be transferred via all interfaces, see Section 8.

FC1_CFG [2:0]	FC1 [15:0]
0	φ_{DLCA}, refer to Section 7.5.4
1	φ_{DLCB}, refer to Section 7.5.4
2	φ_C, refer to Section 7.5.5
3	φ_{DIFF}, refer to Section 7.5.6
4	φ_{CBD}, refer to Section 7.5.7
else	VA, refer to Section 7.5.8

Table 19: Fast Channnel 1 configuration

7.5.9.2 Fast Channel 2 (FC2) with time-multiplexing

The Fast Channel 2 (FC2) additionally allows to change its content over time based on the 2 LSB of the internal rolling counter (RC) as for SENT/SPC or the SPI interface. The Fast Channel 2 can be transferred via interfaces SENT, SPC and SPI and is captured synchronously with FC1.

RC [1:0]	FC2 [15:0]
0	FC2_0
1	FC2_1
2	FC2_2
3	FC2_3

Table 20: Fast Channel 2 time-multiplexing

The FC2 content can be selected by fields FC2_CFG* [2:0] per Table 21. If any of the fields FC2_CFG_RC* is set to zero, the configuration of FC2 for RC time slot 0 (FC2_0) is transmitted. By default, the time-multiplexing is disabled (FC2_CFG_RC1 = FC2_CFG_RC2 = FC2_CFG_RC3 = 0).

FC2_CFG [2:0] FC2_CFG_RC1, FC2_CFG_RC2, FC2_CFG_RC3	FC2_0 [15:0]	FC2_1 [15:0], FC2_2 [15:0], FC2_3 [15:0]
0	φ_{DLCA}, refer to Section 7.5.4	FC2_0 [15:0]
1	φ_{DLCB} , refer to Section 7.5.4	
2	φ_{C}, refer to Section 7.5.5	
3	φ_{DIFF}, refer to Section 7.5.6	
4	φ_{CBD}, refer to Section 7.5.7	
5	VA, refer to Section 7.5.8	
6	SENT/SPC: {4'b0000, SPI_FRFS [3:0] , RC [7:0] }, else: 0	
7	SENT/SPC: Register Probe, refer to Section 8.1.4.1, else: 0	

Table 21: Fast Channel 2 configuration

7.5.10 Signal Conditioning

The MLX90514 is equipped with two signal conditioning units which allow adapting the DSP angles of interest to the output protocol dependent signaling ranges. The two signal conditioning units operate on the selected fast channel values FC1, see Section 7.5.9.1, and FC2, see Section 7.5.9.2. The FC1 signal conditioning is configurable by the 16-bit fields SC1_X1, SC1_X2, SC1_Y1 and SC1_Y2, while the FC2 signal conditioning makes use of SC2_X1, SC2_X2, SC2_Y1 and SC2_Y2 respectively. Figure 12 illustrates the main steps.

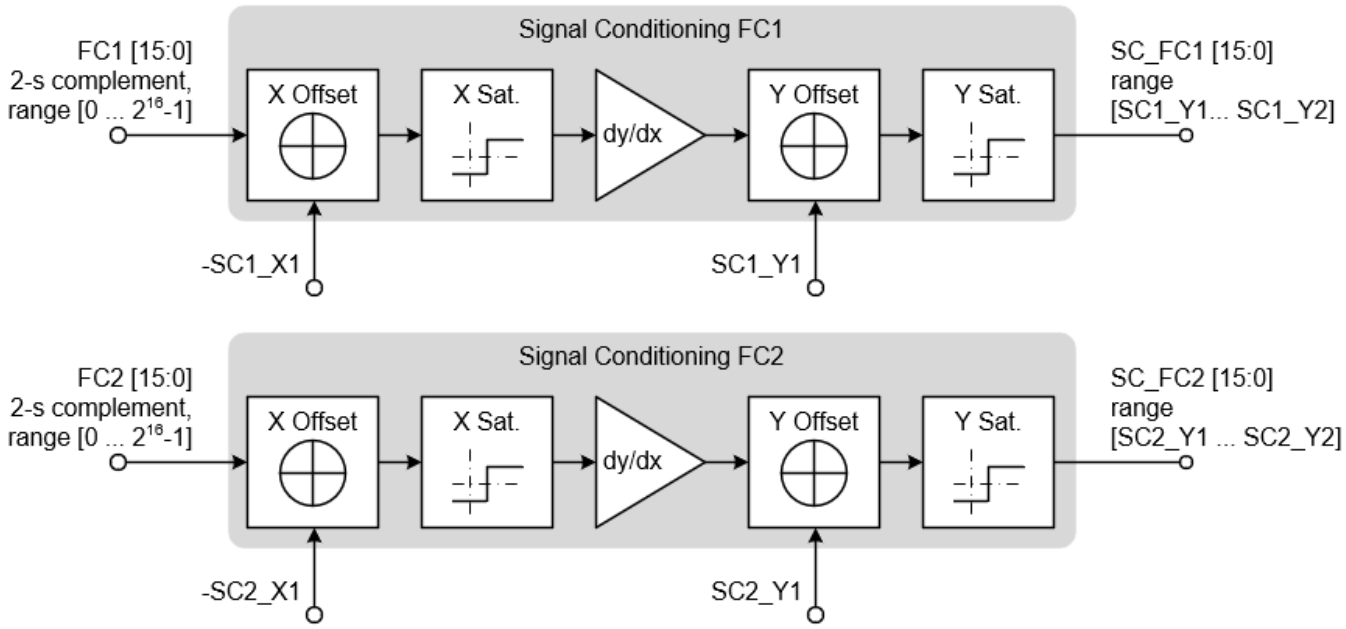


Figure 12: Signal conditioning procedure

The input stage, defined by 2's-complement values SC[1,2]_X1 [15:0], SC[1,2]_X2 [15:0], restricts the angle of interest and saturates all measured angles exceeding the range [SC[1,2]_X1 .. SC[1,2]_X2]. Note that there is no limitation on the value of SC[1,2]_X1 vs SC[1,2]_X2. Input range selection overlapping with the zero-point is possible, e.g. [SC[1,2]_X1 = -8192 (signed) = 57344 (unsigned) , SC[1,2]_X2 = 8191 (signed/unsigned)] selects the electrical angle range [-45 ° .. <45 °].

This stage can be bypassed by setting [SC[1,2]_X1, SC[1,2]_X2] = [0,0] or [0, 2^16-1]. The gain stage scales the signal with the ratio of output range width to the input range width.

The output stage, defined by 2's-complement values SC[1,2]_Y1 [15:0], SC[1,2]_Y2 [15:0], adds the offset SC[1,2]_Y1 and saturates values exceeding the output range [min(SC[1,2]_Y1, SC[1,2]_Y2) ... max(SC[1,2]_Y1, SC[1,2]_Y2)]. It is recommended to understand SC[1,2]_Y1 and SC[1,2]_Y2 here as unsigned values in range [0 .. 2^16-1] and that in the linear transformation SC[1,2]_Y1 refers to SC[1,2]_X1, while SC[1,2]_Y2 refers to SC[1,2]_X2 respectively. This means that if SC[1,2]_X1 < SC[1,2]_X2 but SC[1,2]_Y1 > SC[1,2]_Y2 the transfer characteristic is inverted.

This stage can be bypassed by setting [SC[1,2]_Y1, SC[1,2]_Y2] = [0,0] or [0, 2^16-1].

Within the saturated region, the occurrence of the transition between the SC[1,2]_Y1 and SC[1,2]_Y2 defined outputs can be controlled via the SC1_HL [7:0] and SC2_HL [7:0] parameters. SC[1,2]_HL [7:0] defines the offset of the transition point from the center point (SC[1,2]_X1+SC[1,2]_X2)/2, in units of 360 °/2^8.

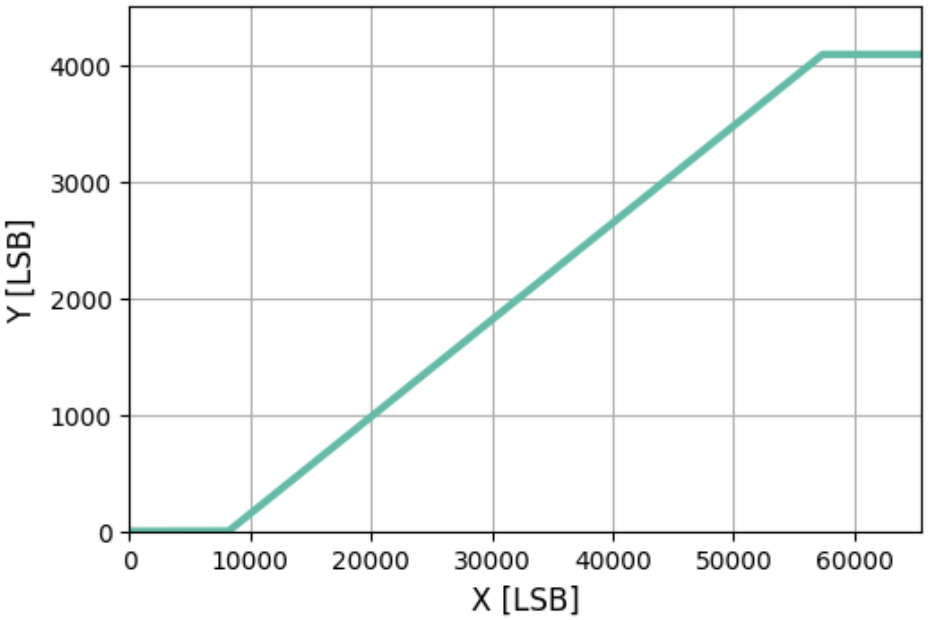


Figure 13: SC transfer curve for FC1 with SC1_X1=8192; SC1_X2=57344; SC1_Y1=1; SC1_Y2=4088, SC1_HL=0

Figure 13 depicts a configuration intended for 12-bit SENT output (valid signal range: [1 .. 4088]) and an input range restriction from 45 ° to -45 ° (span 270 °).

The signal condition transformation influences the signal resolution as follows:

Parameter	Symbol	Resolution	Unit
Resolution of electrical angle	R_{angle_el}	$360/2^{16}$	deg
Resolution of angle after signal conditioning	R_{angle_SC}	$\frac{360}{2^{16}} \cdot \frac{\max(1,\lvert\text{unwrap (SC[1,2]\_X2 - SC[1,2]\_X1)}\rvert)}{\lvert\text{SC[1,2]\_Y2 - SC[1,2]\_Y1}\rvert}$	deg

Table 22: Signal conditioning resolution

The following settings for SC[1,2]_Y1 [15:0], SC[1,2]_Y2 [15:0] are recommended for different output modes to comply to valid signal ranges.

MODE	SC1_Y1 [15:0]	SC1_Y2 [15:0]	SC2_Y1 [15:0]	SC2_Y2 [15:0]	Comment
SENT, H.7	1	65528	1	248	16-bit fast channel 1, 8-bit fast channel 2
SENT, H.6	1	16376	1	1016	14-bit fast channel 1, 10-bit fast channel 2
SENT/SPC, else	1	4088	1	4088	12-bit fast channel 1, 12-bit fast channel 2
PWM	80	T_{FRAME} - 80			minimum pulse width of 4 µs at 20 MHz f_{AC}. Refer to Section 8.4 for other conditions

MODE	SC1_Y1 [15:0]	SC1_Y2 [15:0]	SC2_Y1 [15:0]	SC2_Y2 [15:0]	Comment

Table 23: Signal condition settings for different output modes

The signal values after signal conditioning can be monitored via the register SC_FC1 [15:0] and SC_FC2 [15:0], refer to Section 11.3.

7.5.10.1 Fault band mapping

For functional safety in case of detected errors leading to safe state SS3, the signal conditioning outputs on fast channel 1 the fault band value as defined by field SC1_YE [15:0].

If SC1_YE is configured with a value within the output range (min(SC1_Y1, SC1_Y2) to max(SC1_Y1, SC1_Y2)) or if in case of a missing output range (e.g. SC1_Y1 = SC1_Y2) a fault band reporting is impossible and the MLX90514 switches to the output safe state SS2 (Hi-Z), except for SPI. In SPI (FR), in this case, the data value is transmitted and the safe state information must be transmitted via the enabled frame start byte.

8 Output modes

This chapter describes the output interfaces of the MLX90514. The output mode can be selected with the field PROTOCOL [2:0].

PROTOCOL [2:0]	Output mode	Ordering code
0	SENT	all
1	PWM	all
2	reserved	all
3	SPC	MLX90514GGO-AAA-180-RE
4	SPI	all
else	reserved	all

Table 24: Output mode selection

8.1 Single Edge Nibble Transmission (SENT) SAE J2716

8.1.1 SENT message sequence

In accordance to SENT SAE J2716, the encoding scheme consists of a sequence of pulses which is repeatedly sent by the transmitting module. The transmission consists of the following sequence (all times nominal):

1. Calibration/Synchronization pulse period 56 clock ticks
2. One 4-bit Status and Serial Communication nibble pulse
3. Three to six data nibble pulses according to the basic SENT formats H.1 to H.7, see Section 8.1.3.
4. One 4-bit Checksum nibble pulse.
5. One optional pause pulse

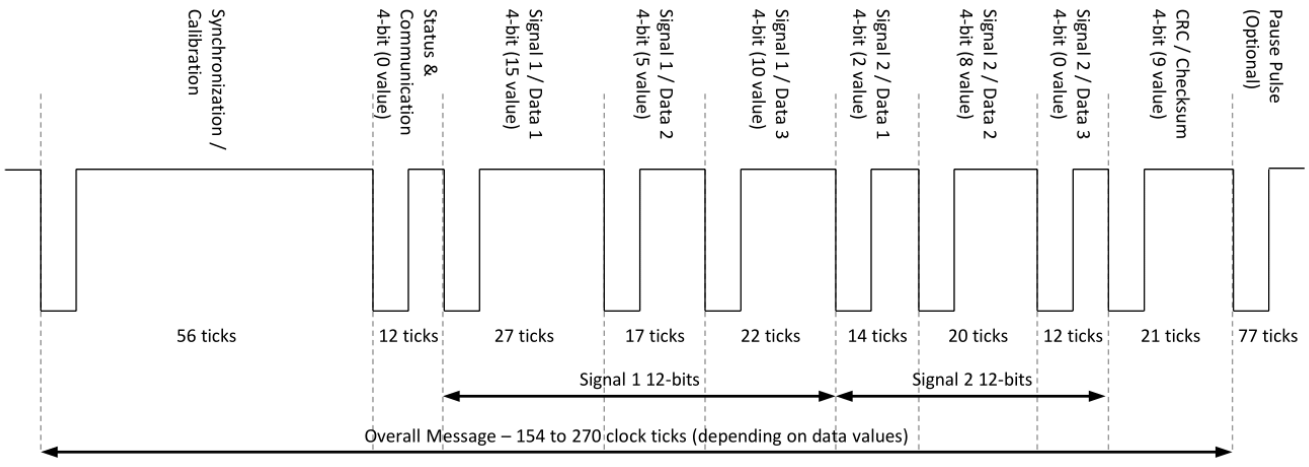


Figure 14: SENT example encoding for two 12-bit signals

The SENT tick times are configurable by field SENT_TICK_TIME [2:0] as follows:

SENT_TICK_TIME [2:0]	T_{tick} [µs], f_{AC} = 20 MHz	T_{tick} [µs], f_{AC} = 10 MHz	T_{tick} [µs], f_{AC} = 5 MHz
0	0.5	0.5	0.6
1	0.75	0.8	0.8
2	1	1	1
3	1.5	1.5	1.6
4	3	3	3
else	6	6	6

Table 25: SENT tick times

Note that for tick times < 1.5 µs the digital pulse shaping mode is required to ensure sufficient bandwidth of the ABE. When the output driver is configured in any of the other non-pulse shaping modulation modes (refer to Section 8.4.1), the SENT nibble shape can be configured using the field SENT_SHAPE_CFG according to Table 26:

SENT_SHAPE_CFG [1:0]	Mode	Condition
0	5 ticks fixed low time	ABE_AOUT_MODE = 1,2,3
1	6 ticks fixed high time	ABE_AOUT_MODE = 1,2,3
2,3	50 % duty cycle	ABE_AOUT_MODE = 1,2,3

Table 26: SENT nibble configuration

The status and communication nibble can be included in the CRC computation by setting the field STATUS_IN_CRC to 1.

8.1.2 Frame period and pause pulse

The optional use of the pause pulse and the frame length in case of its use are controlled by the field T_FRAME [11:0] according to Table 27.

T_FRAME [11:0]	Mode	Frame Length
0	SENT without pause pulse	Message sequence period without pause pulse
> 0	SENT with pause pulse	max ((T_FRAME + 1) · T_{tick} , message sequence period including pause pulse)

Table 27: SENT protocols

Note that ”SENT without pause pulse” maximizes the SENT communication data rate while at the same time preventing equidistant sampling of the (transmitted) sensor data.

8.1.3 SENT frame formats

With field SENT_FC_FORMAT [2:0] all SENT basic frame formats (standard version 2016) are supported.

SENT_FC _FORMAT	Frame Format	Data Nibbles	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6
0, 1 (default)	H.1: Two 12-bit fast channels (CH1, CH2)	6	CH1 [11:8]	CH1 [7:4]	CH1 [3:0]	CH2 [3:0]	CH2 [7:4]	CH2 [11:8]
2	H.2: One 12-bit CH1	3	CH1 [11:8]	CH1 [7:4]	CH1 [3:0]	-	-	-
3	H.3: High-speed with one 12-bit CH1 (3-bit nibbles)	4	CH1 [11:9]	CH1 [8:6]	CH1 [5:3]	CH1 [2:0]	-	-
4	H.4: Secure sensor with 12-bit CH1 and secure sensor information on CH2	6	CH1 [11:8]	CH1 [7:4]	CH1 [3:0]	RC[1] [7:4]	RC[1] [3:0]	~CH1 [11:8]
5	H.5: Single sensor with 12-bit CH1 and zero value on CH2	6	CH1 [11:8]	CH1 [7:4]	CH1 [3:0]	0	0	0
6	H.6: Two fast channels with 14-bit CH1 and 10-bit CH2	6	CH1 [13:10]	CH1 [9:6]	CH1 [5:2]	CH1 [1:0], CH2 [1:0]	CH2 [5:2]	CH2 [9:6]
7	H.7: Two fast channels with 16-bit CH1 and 8-bit CH2	6	CH1 [15:12]	CH1 [11:8]	CH1 [7:4]	CH1 [3:0]	CH2 [3:0]	CH2 [7:4]

Table 28: SENT frame formats

[1] 8-bit rolling counter with rollover back to 0

8.1.4 Fast Channel capturing and encoding

The SENT fast channel 1 (CH1) is mapped to the DSP Fast Channel 1 (FC1), which is configured with FC1_CFG [2:0], see Section 7.5.9.1.

The FC1 signal conditioning output limits SC1_Y1 [15:0] and SC1_Y2 [15:0] should be configured to comply to the reserved signaling ranges according to SENT SAE J2716:

	H.7 (16-bit CH1)	H.6 (14-bit CH1)	else (12-bit CH1)
SC1_Y1 [15:0]	1	1	1
SC1_Y2 [15:0]	65528	16376	4088

Table 29: SENT FC1 reserved signaling ranges

Further restrictions of the output range are optional.

In SENT mode the DSP angular values after signal conditioning / interpolation are captured into CH1 with falling edge of the SYNC pulse and after an adjustable capture delay defined by field SENT_FC1_CPT_DLY [6:0] [ticks], see Figure 15. It is not recommended to program SENT_FC1_CPT_DLY to capture time later than the SCN nibbles, unless the captured value shall be transmitted with the next SENT frame.

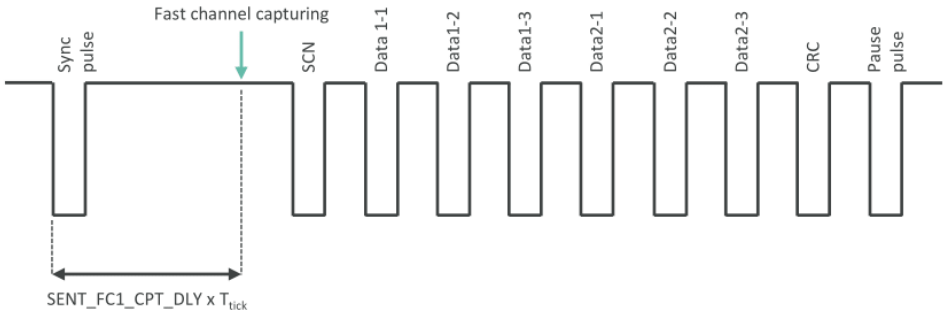


Figure 15: SENT fast channel capturing timing

In dual-channel modes H.1, H.6, H.7, the SENT fast channel 2 (CH2) is mapped to the DSP Fast Channel 2 (FC2), which is configured with FC2_CFG [2:0] and others, see Section 7.5.9.2. The FC2 data are acquired synchronously to the FC1 data.

The FC2 signal conditioning output limits SC2_Y1 [15:0] and SC2_Y2 [15:0] should be configured to comply to the reserved signaling ranges according to SENT SAE J2716:

	H.1 (12-bit CH2)	H.6 (10-bit CH2)	H.7 (8-bit CH2)
SC2_Y1 [15:0]	1	1	1
SC2_Y2 [15:0]	4088	1016	248

Table 30: SENT FC2 reserved signaling ranges

8.1.4.1 Register Probe

If FC2_CFG [2:0] is set to 7 (Register probe), the CH2 transmits the content of a register or memory address, which is specified by SENT_FC2_ADR [7:0]. The byte aligned address (see Section 11) maps to 16-bit word aligned value for SENT_FC2_ADR [7:0] by omitting the LSB, e.g. address 72 (TEMP) is configured by SENT_FC2_ADR = 36.

The selected 16-bits register can be transmitted over two successive frames with two different offsets, programmable via SENT_FC2_OFS0 [3:0] (rolling counter LSB (RC[0]) = 0) and SENT_FC2_OFS1 [3:0] (rolling counter LSB (RC[0])= 1).

8.1.5 Startup behavior

After start-up and after leaving safe state SS2 the circuit will send initialization frame(s) with fast channel 1 (CH1) content chosen by bit SENT_INIT_GM:

SENT_INIT_GM	CH1 initialization value	Comment
0	0	SAE compliant
1	SC1_YE	OEM compliant

Table 31: SENT initialization frame value

In frame format H.4 the startup behavior of the 8-bit rolling counter (RC) can be configured by bit SENT_RC_INIT as follows:

SENT_RC_INIT	Description
0	Rolling counter = 0 during the initialization frame(s)
1 (default)	Rolling counter increments during initialization frame(s)

Table 32: Rolling counter initialization

8.1.6 Serial Message channel (slow channel)

Serial data is transmitted sequentially in bit number 3 and 2 of the status and communication nibble. A serial message frame stretches over 18 consecutive SENT data messages from the transmitter.

8.1.6.1 Enhanced Serial Message (ESM)

The MLX90514 supports enhanced serial messages with 12-bit data and 8-bit message ID (SAE J2716 APR2016 5.2.4.2, Figure 5.2.4.2-1) if bit SENT_SC_FORMAT is set to 1. According to the standard, Serial Data bit # 2 contains a 6-bits CRC followed by a 12-bits data. The message content is defined by a 8-bit message ID transmitted by the Serial Data bit # 3.

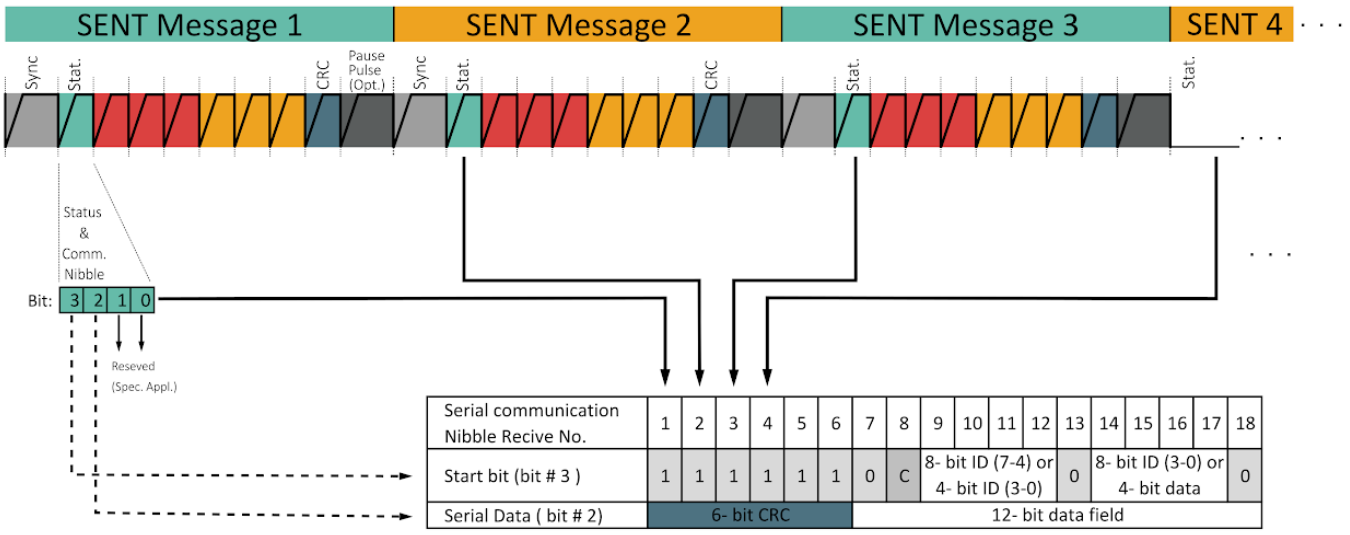


Figure 16: Enhanced serial message

By default, a sequence consisting of a cycle of 26 data is transmitted. An extended sequence can be configured with bit SENT_SLOW_EXTENDED set to 1. If bit SENT_SC_FORMAT = 1 and bit SENT_SLOW_EXTENDED = 0, the following sequence of enhanced serial messages is transmitted.

#	8-bit ID	Definition	Value (12-bit)
1	0x01	Diagnostic error code	ESM status code
2	0x06	SENT standard revision	{8'd0, SENT_REV[3:0]}
3	0x01	Diagnostic error code	ESM status code
4	0x05	Manufacturer code	SENT_MAN_CODE
5	0x01	Diagnostic error code	ESM status code
6	0x03	Channel 1 / 2 Sensor type	SENT_SENSOR_TYPE
7	0x01	Diagnostic error code	ESM status code
8	0x07	Fast channel 1: X1	SC1_X1[15:4]
9	0x01	Diagnostic error code	ESM status code
10	0x08	Fast channel 1: X2	SC1_X2[15:4]
11	0x01	Diagnostic error code	ESM status code
12	0x09	Fast channel 1: Y1	H.6: SC1_Y1[13:2], H.7: SC1_Y1[15:4], else: SC1_Y1[11:0]
13	0x01	Diagnostic error code	ESM status code
14	0x0A	Fast channel 1: Y2	H.6: SC1_Y2[13:2], H.7: SC1_Y2[15:4], else: SC1_Y2[11:0]
15	0x01	Diagnostic error code	ESM status code
16	0x23	(Internal) temperature	Current temperature
17	0x01	Diagnostic error code	ESM status code
18	0x29	Sensor ID #1	SENT_SENSOR_ID1
19	0x01	Diagnostic error code	ESM status code
20	0x2A	Sensor ID #2	SENT_SENSOR_ID2
21	0x01	Diagnostic error code	ESM status code
22	0x2B	Sensor ID #3	SENT_SENSOR_ID3
23	0x01	Diagnostic error code	ESM status code
24	0x2C	Sensor ID #4	SENT_SENSOR_ID4
25	0x01	Diagnostic error code	ESM status code
26	0x24	Signal strength indicator	{4'd0, SSI [7:0]}

Table 33: SENT enhanced serial message sequence

If bit SENT_SLOW_EXTENDED is set to 1, the sequence of enhanced serial messages is extended as follows.

#	8-bit ID	Definition	Value (12-bit)
27	0x01	Diagnostic error code	ESM status code
28	0x90	OEM Code #1	SENT_OEM_CODE1
29	0x01	Diagnostic error code	ESM status code
30	0x91	OEM Code #2	SENT_OEM_CODE2
31	0x01	Diagnostic error code	ESM status code
32	0x92	OEM Code #3	SENT_OEM_CODE3
33	0x01	Diagnostic error code	ESM status code
34	0x93	OEM Code #4	SENT_OEM_CODE4
35	0x01	Diagnostic error code	ESM status code
36	0x94	OEM Code #5	SENT_OEM_CODE5
37	0x01	Diagnostic error code	ESM status code
38	0x95	OEM Code #6	SENT_OEM_CODE6
39	0x01	Diagnostic error code	ESM status code
40	0x96	OEM Code #7	SENT_OEM_CODE7
41	0x01	Diagnostic error code	ESM status code
42	0x97	OEM Code #8	SENT_OEM_CODE8

Table 34: SENT enhanced serial message extended sequence

8.1.6.2 Short Serial Message (SSM)

The MLX90514 supports short serial messages with 8-bit data and 4-bit message ID (SAE J2716 APR2016 5.2.4.2, Figure 5.2.4.1-1) if bit SENT_SC_FORMAT is set to 0. According to the standard, Serial Data bit # 2 contains a 4-bit message ID followed by an 8-bit message content and a 4-bit CRC.

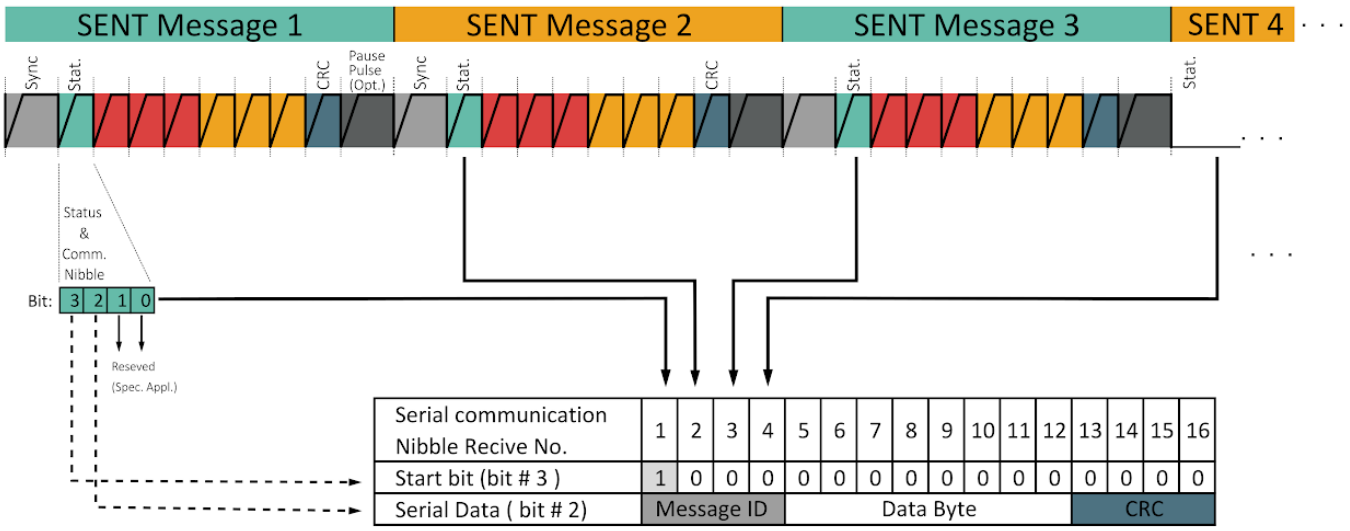


Figure 17: Short serial message

The following sequence of 26 data bytes is transmitted:

#	4-bit ID	Definition	Value (8-bit)
1	0x01	Diagnostic error code	SSM status code
2	0x06	SENT standard revision	{4'd0, SENT_REV[3:0]}
3	0x01	Diagnostic error code	SSM status code
4	0x05	Manufacturer code	SENT_MAN_CODE[11:4]
5	0x01	Diagnostic error code	SSM status code
6	0x03	Channel 1 / 2 Sensor type	SENT_SENSOR_TYPE[11:4]
7	0x01	Diagnostic error code	SSM status code
8	0x07	Fast channel 1: X1	SC1_X1[15:8]
9	0x01	Diagnostic error code	SSM status code
10	0x08	Fast channel 1: X2	SC1_X2[15:8]
11	0x01	Diagnostic error code	SSM status code
12	0x09	Fast channel 1: Y1	H.6: SC1_Y1[13:6], H.7: SC1_Y1[15:8], else: SC1_Y1[11:4]
13	0x01	Diagnostic error code	SSM status code
14	0x0A	Fast channel 1: Y2	H.7: SC1_Y2[13:6], H.7: SC1_Y2[15:8], else: SC1_Y2[11:4]
15	0x01	Diagnostic error code	SSM status code
16	0x02	(Internal) temperature	Current temperature
17	0x01	Diagnostic error code	SSM status code

#	4-bit ID	Definition	Value (8-bit)
18	0x0B	Sensor ID #1	SENT_SENSOR_ID1[11:4]
19	0x01	Diagnostic error code	SSM status code
20	0x0C	Sensor ID #2	SENT_SENSOR_ID2[11:4]
21	0x01	Diagnostic error code	SSM status code
22	0x0D	Sensor ID #3	SENT_SENSOR_ID3[11:4]
23	0x01	Diagnostic error code	SSM status code
24	0x0E	Sensor ID #4	SENT_SENSOR_ID4[11:4]
25	0x01	Diagnostic error code	SSM status code
26	0x04	Signal strength indicator	SSI

Table 35: SENT short serial message sequence

8.1.7 SSM and ESM Status Code

The 8-bit short serial message status code (SSM_SC), reporting safe state SS3, indicates faults as follows:

	SSM_SC [7:0]	Diagnostic	Description
	00h		No error
Common failures			
	01h	DIAG_LC_P_LO	LCO period too low
	02h	DIAG_LC_P_HI	LCO period too high
	03h	DIAG_TEMP_LO	Temperature too low
	04h	DIAG_TEMP_HI	Temperature too high
	05h	DIAG_DSP	DSP error
Channel A failures			
	90h	DIAG_SL_A	Sensor loss
	91h	DIAG_SS_A	Sensor short
	92h	DIAG_AGC_HI_A or DIAG_SSI_LO_A	Signal too low
	93h	DIAG_AGC_LO_A or DIAG_SSI_HI_A	Signal too high
	94h	DIAG_ACC_A	Rotational acceleration too high
	95h	DIAG_SPEED_A	Rotation too fast
Channel B failures			
	A0h	DIAG_SL_B	Sensor loss

	SSM_SC [7:0]	Diagnostic	Description
	A1h	DIAG_SS_B	Sensor short
	A2h	DIAG_AGC_HI_B or DIAG_SSI_LO_B	Signal too low
	A3h	DIAG_AGC_LO_B or DIAG_SSI_HI_B	Signal too high
	A4h	DIAG_ACC_B	Rotational acceleration too high
	A5h	DIAG_SPEED_B	Rotation too fast
Digital backend failures			
	B2h	DIAG_VERNIER	Vernier reserve error

Table 36: SENT short serial message status

The mapping reported in Table 36 forms a priority encoding from top to bottom. The SSM status code equal to 0 indicates normal operation (no error).

The 12-bit enhanced serial message status code (ESM_SC), reporting safe state SS3, derived from SSM_SC with as per Table 37.

SSM_SC	ESM_SC
0	0
> 0	0x800 + SSM_SC

Table 37: Enhanced serial message status code

8.2 Short PWM code (SPC)

The MLX90514 supports the SPC extension to enable the following features overcoming SENT limitations:

- Synchronous transmissions, whereby the master initiates the transfer
- Exact data sampling point
- Constant sampling interval, triggered by the ECU
- Bidirectional functionality to allow bus systems
- Improved data integrity and diagnosis methods, including a more efficient checksum algorithm beside several CRC methods

The physical layer properties of transmission in SPC mode are equivalent to Single Edge Nibble Transmission (SENT) SAE J2716. The SPC mode is activated with PROTOCOL [2:0] set to 3.

8.2.1 SPC frame formats

The MLX90514 supports all frame formats according to SPC, see Figure 18 for all the possible SPC configurations.

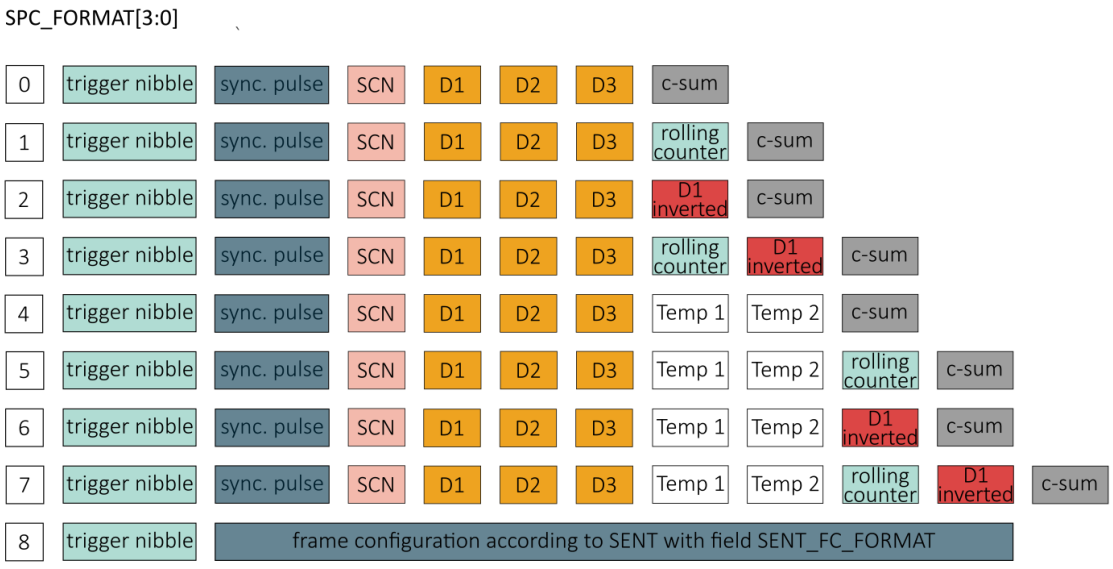


Figure 18: SPC configurations

Fast channel 1 (CH1, 12 bit) data is transmitted with most significant nibble first (D1: MSN;D2: MidN; D3: LSN). Temp1 and Temp2 refers to the fast channel 2 (CH2) 8-bit temperature value according to SENT.

The MLX90514 implements a 4-bits SPC rolling counter which is updated on every frame transmitted, also in case the sensor is determined to be in error condition and also when the frame content with the application layer data is not updated. The rolling counter initialization is controlled by the SENT_RC_INIT as per Table 32.

The SPC frame format can be selected with the following fields:

- SPC_FORMAT [3:0] to select the content of the data nibbles (see Figure 18 : D1 .. D3, Temp 1..2, rolling counter, D1 inverted). With SPC_FORMAT set to 8 frame formats according to the SENT standards are still possible and can be used for compatibility reasons.

SPC_FORMAT [3:0]	SPC format
0 (default)	CH1 + c-sum
1	CH1 + rolling_counter + c-sum
2	CH1 + D1 inverted + c-sum
3	CH1 + rolling_counter + D1 inverted + c-sum
4	CH1 + temp(2 nibbles) + c-sum
5	CH1 + temp(2 nibbles) + rolling_counter + c-sum
6	CH1 + temp(2 nibbles) + D1 inverted+ c-sum
7	CH1 + temp(2 nibbles) + rolling_counter + D1 inverted + c-sum
8	frame configuration according to [SENT] with field SENT_FC_FORMAT[2:0], see Section 8.1.3 [1]

Table 38: SPC format selection

- ID_IN_STATUS to define the SCN field (SENT status & communication nibble)

ID_IN_STATUS	SCN field status
0 (default)	the two slow-message bits are as described in the SENT SAE standard
1	the two slow-message bits are replaced in all cases by the 2-bit chip ID

Table 39: SCN field status selection

- If ID_IN_STATUS = 1, field SPC_SCN_BIT_ORDER defines the bit order in the SCN field:

Figure 19: SCN bit order options

- SPC_CSUM_MODE[1:0] to select the fields for the checksum (CRC) computation

SPC_CSUM_MODE [1:0]	Checksum calculation range
0 (default)	Data nibbles
1	Data nibbles + ID
2	Data nibbles + Rolling Counter
3	Data nibbles + ID + Rolling Counter

Table 40: SPC CRC computation selection

The checksum (CRC) calculation method can be selected via the SPC_CSUM_CFG [1:0] field:

SPC_CSUM_CFG [1:0]	Method
0, 1	SAE standard (SENT J2716 specification)
2	SPC Method “O”: check sum is a modulo-16 sum of nibble values, where each second nibble value sign is inverted
3	SPC method ”E”: having the simple sum as the MSB and the alternating sum as LSB

Table 41: SPC CRC calculation method

8.2.2 SPC bus line handling and synchronous transmission

SPC uses a master trigger pulse, which initiates the data transmission from the slave. The master trigger pulse and its position within an SPC frame is depicted in Figure 20.

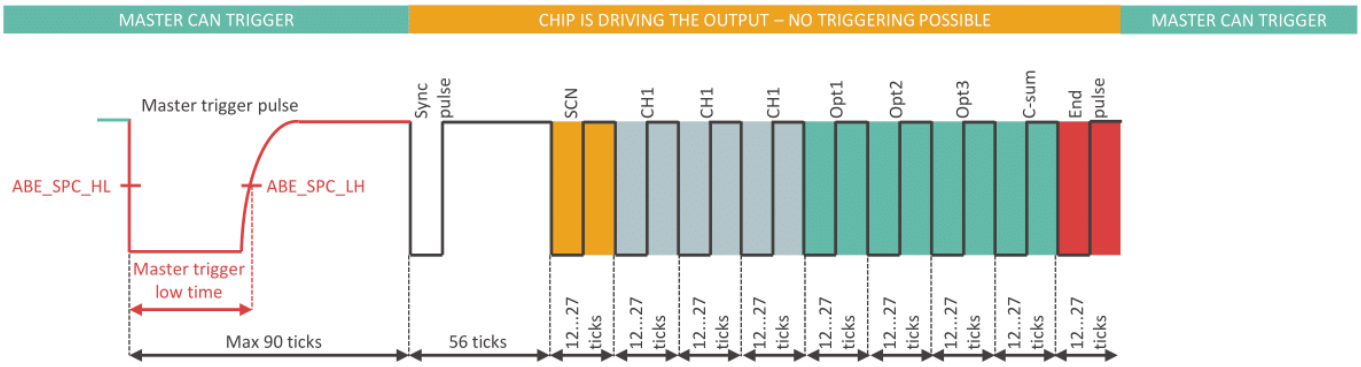


Figure 20: SPC frame example highlighting the master trigger pulse

The MLX90514 allows to control SPC bus modes with field SPC_TRIGGER_MODE [1:0] as follows

SPC_TRIGGER_MODE [1:0]	SPC trigger mode
0	Synchronous point-to-point
1 (default)	Bus mode w/ constant length trigger pulse
2	Bus mode w/ variable length trigger pulse
3	Bus mode w/ fully overlapping trigger pulse

Table 42: SPC trigger modes

If SPC_TRG_TIME [6:0] = 0, the master trigger pulse duration is defined by the selected trigger modes as detailed in Figure 21. Otherwise, the master pulse duration can directly be programmed to SPC_TRG_TIME [ticks].

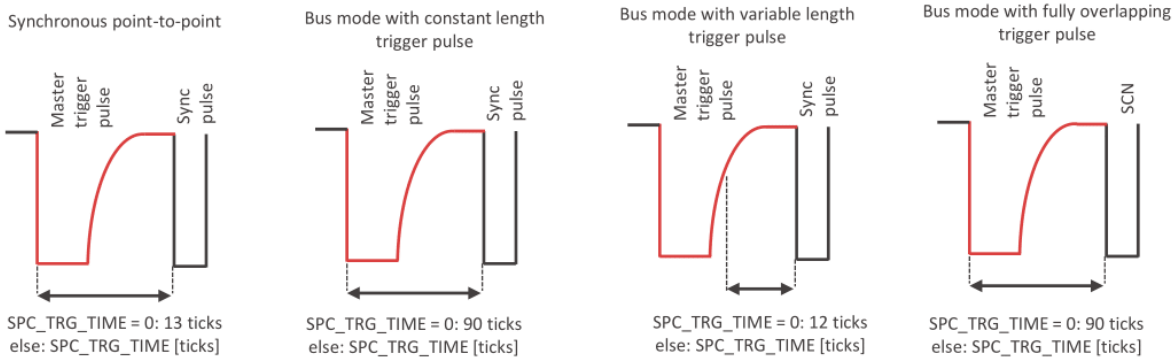


Figure 21: SPC master trigger pulse duration

The protocol transfer is started after detection of a valid master low time as per Table 43. The threshold voltages for the detection of the falling and rising edge are detailed in Table 44. In SPC bus modes, a response frame is transmitted only if the received master trigger low time matches to the one corresponding to the configured chip ID as defined by CUS_CHIP_ID [1:0]. The fields SPC_TRIGLL_OFS0 [3:0], SPC_TRIGLL_OFS1 [3:0], SPC_TRIGLL_OFS2 [3:0], SPC_TRIGLL_OFS3 [3:0] can be used to tune the length of the valid master trigger low time. The SPC bus modes allow a parallel connection of up to 4 sensors on a common bus line.

SPC_TRIGGER_MODE	CUS_CHIP_ID	Min [tcks]	Typ	Max [tcks]
0	n/a	2 + SPC_TRIGLL_OFS0		5 + SPC_TRIGLL_OFS1
>= 1	0	8 + SPC_TRIGLL_OFS0		15 + SPC_TRIGLL_OFS1
	1	16 + SPC_TRIGLL_OFS1		28 + SPC_TRIGLL_OFS2
	2	29 + SPC_TRIGLL_OFS2		49 + SPC_TRIGLL_OFS3
	3	50 + SPC_TRIGLL_OFS3		82

Table 43: SPC master low time detection windows

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Master trigger pulse falling edge detection threshold	ABE_SPC_HL	1.0	1.15	1.4	V	
Master trigger pulse raising edge detection threshold	ABE_SPC_LH	1.1	1.35	1.5	V	
Master trigger pulse detection threshold hysteresis	ABE_SPC_Hyst	0.1	0.2	0.3	V	

Table 44: SPC master trigger pulse edges detection thresholds

After the reception of an invalid trigger pulse (e.g. non-matching ID), the reception of further master trigger pulses is suppressed for a configurable time defined by the field SPC_BLANK_TIME [8:0], in [ticks].

8.2.3 SPC Rx-Tx transition timing

In SPC mode, during Rx mode (master pulse period), the OUT pin is in Hi-Z, while during Tx mode (frame transmission) it operates according to the ABE_AOUT_MODE [2:0] settings. The timing of the Hi-Z phase is defined by the SPC_OUT_ON_DLY [6:0] and SPC_OUT_OFF_DLY [8:0] fields as per Table 45 and Table 46.

SPC_OUT_ON_DLY [6:0]	Description
0	Hi-Z to TX transition at frame start (sync pulse falling edge)
> 0	Hi-Z to TX transition at SPC_OUT_ON_DLY ticks after master pulse falling edge, but only if master pulse is validated

Table 45: SPC Hi-Z to Tx mode transition timing

SPC_OUT_ON_DLY [6:0]	Description
0	TX to Hi-Z transition at end of (minimum length) pause pulse
> 0	TX to Hi-Z transition at SPC_OUT_OFF_DLY ticks after frame start (sync pulse falling edge)

Table 46: SPC Tx to Hi-Z mode transition timing

8.2.4 SPC fast channels capturing

In SPC bus modes, data capturing is enabled only if the received master trigger pulse ID matches to the configured SPC_MEAS_ID [1:0]. This allows combining synchronized measurements with sequential data transfer on the joined bus. The rationale is that the ECU has the possibility to trigger the measurement at the same time for

different sensors on the bus. The ”Measurement ID” is intended to synchronize the measurement acquisition. Having a transmission buffer can support this need.

In SPC mode, angular values after signal conditioning / interpolation are captured into CH1 and CH2 with falling edge of the master trigger pulse or the SYNC pulse, depending on bit SPC_FC1_CPT_MST. An adjustable delay is controlled as in SENT mode by field SENT_FC1_CPT_DLY [6:0] [ticks].

SPC_FC1_CPT_MST	Capture timing
0 (default)	falling edge of SYNC pulse + SENT_FC1_CPT_DLY
1	falling edge of master trigger pulse + SENT_FC1_CPT_DLY

Table 47: Capture timing selection

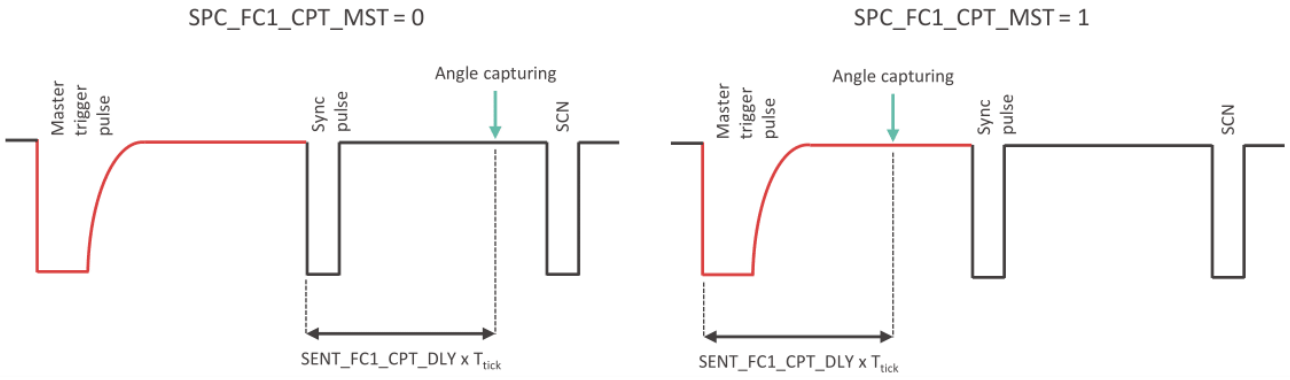


Figure 22: SPC fast channel capturing timing

It is not recommended to program SENT_FC1_CPT_DLY to capture time later than the SCN nibbles, unless the captured value shall be transmitted with the NEXT SENT frame.

8.3 Pulse Width Modulation (PWM)

If PROTOCOL [2:0] is set to 1, the MLX90514 performs pulse width modulation (PWM) output with a time resolution of $1/f_{AC}$. The value transmitted is the one selected by the SENT_FC1 field, refer to Sec. 11.1.4.

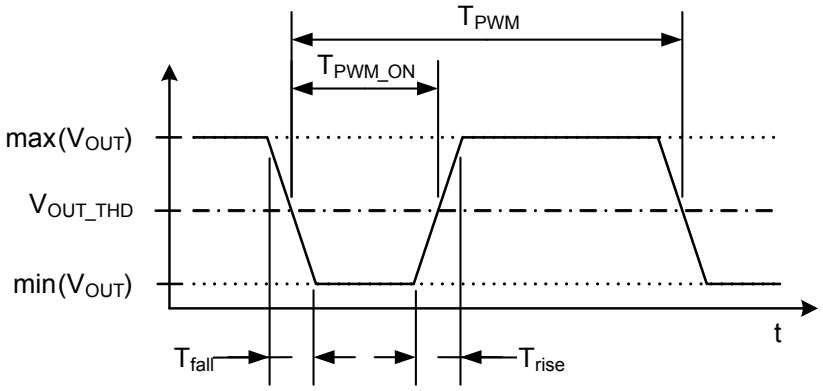


Figure 23: PWM signal definitions

The PWM total period T_{PWM} is configured by the frame length parameter T_FRAME [15:0] and depends on the application clock frequency f_{AC}:

$$T_{PWM} = \frac{\text{T\_FRAME [15:0]}}{f_{AC}}$$

The PWM pulse duration T_{PWM_ON} is proportional to the angular value after signal conditioning (φ_{SC}) and interpolation, captured at the beginning of the PWM period:

$$T_{PWM\_ON} = \frac{\text{SC\_FC1 [15:0]}}{f_{AC}}$$

As a consequence, the lower and upper limit of the PWM pulse duration as well as the fault band value are defined by SC1_Y1, SC1_Y2 and SC1_YE respectively, see Section 7.5.10. This implies that T_{PWM} must be greater/equal to the maximum pulse duration defined by the signal conditioning. This is achieved on the following condition:

$$\text{T\_FRAME} > \max(\text{SC1\_Y1, SC1\_Y2, SC1\_YE})$$

Note that the finite rise/fall times (see Section 8.4) constrain the minimum and maximum pulse durations. Exceeding the maximum and minimum pulse duration is prevented by respecting the following formulas:

$$\min(\text{SC1\_Y1, SC1\_Y2, SC1\_YE}) \geq \max(T_{rise}, T_{fall}) \cdot f_{AC}$$
$$\max(\text{SC1\_Y1, SC1\_Y2, SC1\_YE}) \leq \text{T\_FRAME} - \max(T_{rise}, T_{fall}) \cdot f_{AC}$$

The polarity of the PWM pulse can be adjusted with bit SENTPWM_INV. If SENTPWM_INV = 0 (default), the low-state duration is proportional to the transmitted data (T_{PWM_ON}), else the high-state respectively.

8.3.1 PWM performance characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
PWM output resolution	R_{PWM}		12	16	bit	
PWM frequency tolerance	df_{PWM}	-3.5		3.5	%	
PWM frequency range	f_{PWM}	100		5000	Hz	f_{AC} adapted
PWM duty cycle jitter [1]	J_{DC}	-0.02		0.02	%	
PWM period jitter [1]	J_{PWM}	-500		500	ns	
PWM T_{ON} drift				500	ns	ABE_AOUT_MODE = 3 ABE_AOUT_SR = 0
PWM T_{ON} offset		-1.5		1.5	µs	ABE_AOUT_MODE = 3 ABE_AOUT_SR = 0

Table 48: PWM characteristics

1] ±3σ values

To compensate for mismatches between the rising and falling edge delays, the field PWM_DC_OFS [8:0] (signed) can be used to adjust the T_{PWM_ON} time by adding to T_{PWM_ON} a systematic offset ΔT_{PWM_ON} according to the following formula:

$$\Delta T_{PWM\_ON} = \frac{PWM\_DC\_OFS[8:0]}{f_{AC}}$$

The corresponding value measured by DIAG_PWM can be read from DSP register DIAG_PWM_DC_OFS [8:0].

8.4 Physical layer output configuration (PWM / SENT / SPC modes)

The MLX90514 OUT driver can be configured with field ABE_AOUT_MODE [2:0] as per Table 49.

ABE_AOUT_MODE [2:0]	OUT operation
0	reserved
1	binary modulation with open-drain-NMOS
2	binary modulation with open-drain-PMOS
3	binary modulation with push-pull
4 (default)	digital pulse-shaping with improved emissions, 5 V amplitude
5	digital pulse-shaping with improved emissions, 3.3 V amplitude

Table 49: OUT mode selection

The resistive load on pin OUT, e.g. the external pull-up or pull-down resistor should be carefully selected, because the MLX90514 has a built-in high order low pass filter. A large resistive load will deteriorate the generated SENT/SPC signal, and could make the output signal not comply to the SENT/SPC specifications, such as the fall times and the minimum output voltages. The values in Table 62 should be considered, which means it is not recommended to have a resistive load value smaller than 10 kΩ, and a resistive load value smaller than 3 kΩ should be avoided. The maximum output resistive load value should be less than 55 kΩ to avoid unexpected impact from leakage current.

Furthermore, the output capacitance should also be properly chosen, together with the output resistive load to correspondingly match the application, e.g. tick time, to allow appropriate time constant for the transmission of the SENT/SPC signal.

8.4.1 Open Drain and Push-Pull Mode

The following table for rise (T_{rise}) and fall (T_{fall}) times refer to the binary driven output modes (ABE_AOUT_MODE [2:0] in [1,2,3]). The rise/fall times for the digital pulse-shaped mode (ABE_AOUT_MODE = 4, 5) are listed in Section 8.4.2. Slower rise/fall times are achieved by setting ABE_AOUT_SR to 1.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Rise time	T_{rise_pp}	1.0	2.0	4.0	µs	ABE_AOUT_MODE = 2, 3 ABE_AOUT_SR = 0, C_{OUT} < 10 nF, step 30 % - 70 % of VS
Fall time	T_{fall_pp}	1.0	2.0	4.0	µs	ABE_AOUT_MODE = 1, 3 ABE_AOUT_SR = 0, C_{OUT} < 10 nF, step 70 % - 30 % of VS

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Slow Rise Time	$T_{rise\_pp\_slow}$	2.0	3.5	5.5	µs	ABE_AOUT_MODE = 3 ABE_AOUT_SR = 1, C_{OUT} < 15 nF, step 30 % - 70 % of VS
Slow Fall Time	$T_{fall\_pp\_slow}$	2.0	3.5	5.5	µs	ABE_AOUT_MODE = 3 ABE_AOUT_SR = 1, C_{OUT} < 15 nF, step 70 % - 30 % of VS
Fall Time NMOS open-drain mode	T_{fall_od}	4.0	7.5	15.0	µs	ABE_AOUT_MODE = 1, C_{OUT} = 10 nF, R_{PU} = 10 kOhm, VS_PU = 18 V, step 30 % - 70 % of VS_PU

Table 50: Rise and fall time for open drain and push-pull modes

8.4.2 Digital Pulse Shaping

With ABE_AOUT_MODE = 4,5 the MLX90514 supports digital pulse shaping for binary modulation modes for improved EMC emissions and reduced dependency on external load components. For ABE_AOUT_MODE = 4, the output voltage range is 5 V, while for ABE_AOUT_MODE = 5 the output voltage range is 3.3 V. The slope of the pulse shaping is dependent on SENT_TICK_TIME [2:0] as per Table 51. For SENT/SPC the pulse shaping defines the nibble falling and rising slopes, with rise time slower than fall time. In PWM mode the pulse shape on rising and falling edge are inverse and symmetrical around VS/2 and leading to equal rise and fall time. Pulse shaping does not influence duty cycle and period of the modulation when measured at VS/2. The MLX90514 internally compensates for digital processing delays of the pulse shaping.

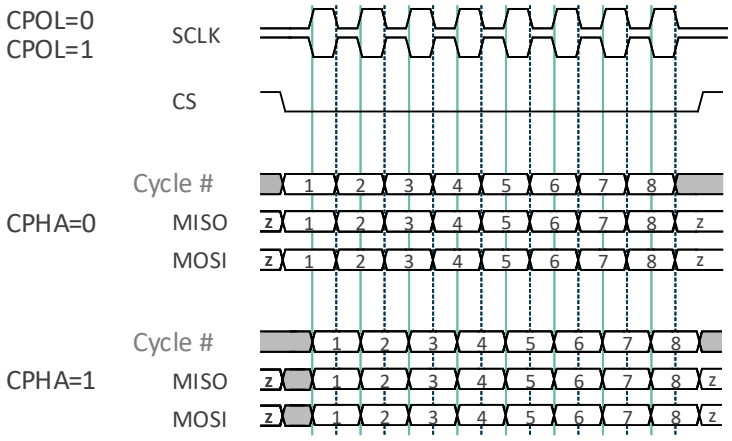
SENT_TICK_TIME	SENT Fall Time [µs] 90 % to 10 %	SENT Rise Time [µs] 10 % to 90 %	PWM Fall/Rise Time [µs] 10 % to 90 %	ABE_ABOUT_SR
0, 1	1.0	2.2	1.0	0
2	2.0	4.4	2.0	1
3	3.0	6.6	3.0	1
4	6.0	13.2	6.0	1
else	12.0	26.4	12.0	1

Table 51: Rise and fall time for pulse shaping mode

8.5 Serial Peripheral Interface (SPI)

The MLX90514 features a full-duplex slave high-speed SPI for sensor data transfer and device programming. An SPI transmission can be started with the active-low pin CS and will override any other configured output interface. However, with PROTOCOL [2:0] = 4 the SPI mode operates exclusively.

All standard SPI timing modes are supported by field SPI_MODE [1:0].



SPI_MODE [1:0]	Clock polarity (CPOL)	Clock phase (CPHA)
0	0	0
1	0	1
2	1	0
3	1	1

Table 52: SPI timing mode

8.5.1 SPI transactions

The SPI supports memory and register read / write access and continuous readout with functional safety protections which can be synchronized over multiple slaves.

Transaction are started with a command byte from MOSI, see Table 53.

Command	Command code	Description
RD	6'b110011	Register Read, see Section 8.5.1.1
WR	6'b011110	Register Write, see Section 8.5.1.2
FR	6'b000000	Frame Read, see Section 8.5.1.3
SFR	6'b110100	Super Frame Read, see Section 8.5.1.4

Table 53: SPI commands

In case of receiving an invalid command byte the IC defaults to sensor data transfer (FR). If MISO does not carry data, it returns the previous MOSI byte denoted as MOSI(k-1).

The SPI protocol comprises the MSB-1st byte-wise basic transactions “Register Read” (RD), “Register Write” (WR) and “Frame Read” (FR), see Figure 24. Each line depicts an SPI byte transfer on MISO and MOSI respectively. Unused values from MOSI are not displayed. Greyed fields are optional.

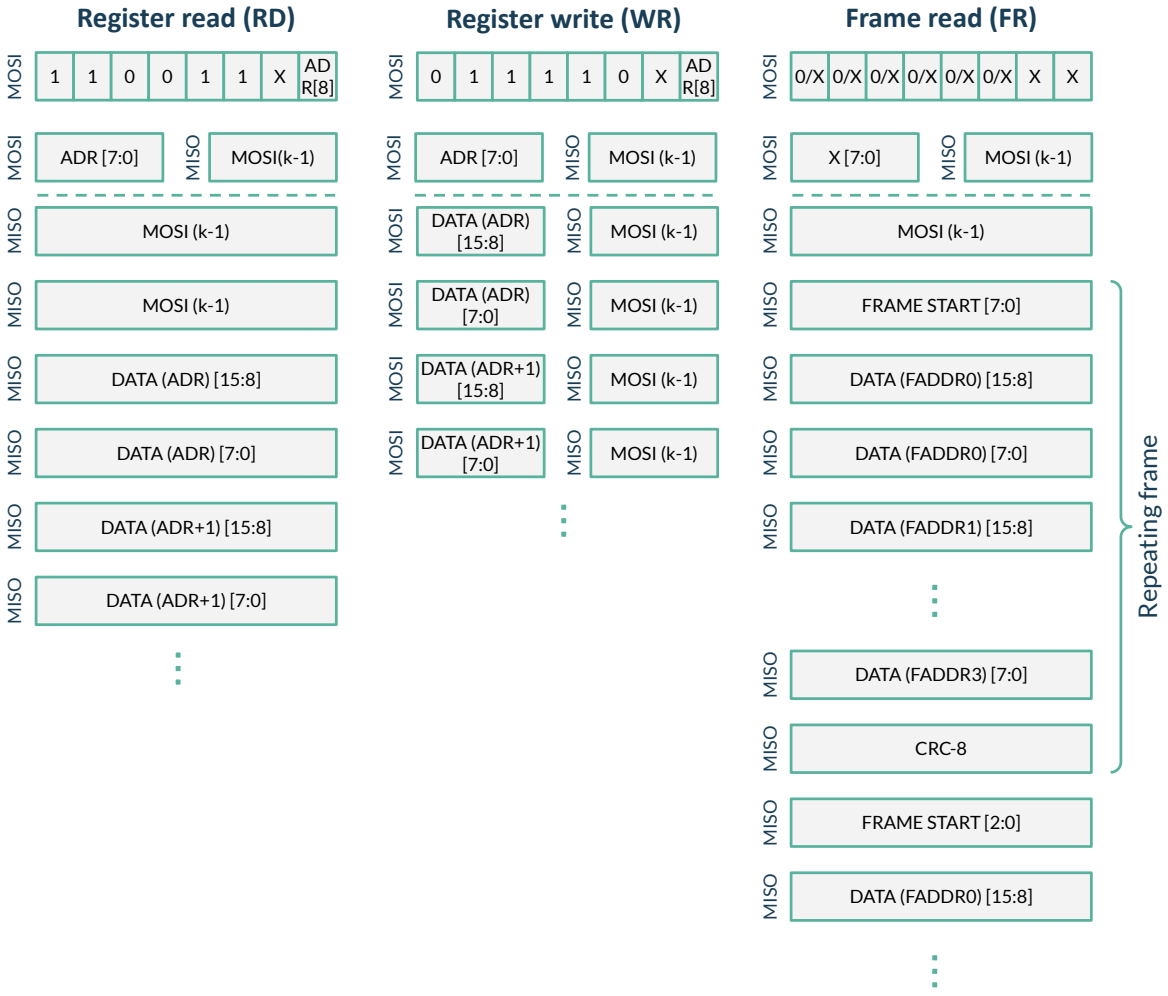


Figure 24: MLX90514 basic SPI transactions

8.5.1.1 Register Read (RD)

”Register Read” (RD) allows DMA read access to device registers or memory, starting from the 16-bit word aligned address {A8, ADR [7:0], 1'b0}, which covers the complete IC address range including EEPROM. With SPI_DMY [0] = 1 an additional delay byte can be introduced which allows adjusting the word alignment of the data transfer.

The RD command features auto-address-increment, which allows to read out a sequence of registers as long as CS remains in active state.

8.5.1.2 Register Write (WR)

”Register Write” (WR) allows DMA write access to device registers or memory, starting from the 16-bit word aligned address {A8, ADR [7:0], 1'b0}, which covers the complete IC address range including EEPROM.

While the 16-bit write data per address is transmitted in 2 bytes on MOSI, the previous transfer can be verified with MISO (k-1). Note that this data is the content of the SPI shift register, not the content of the target address.

The WR command features auto-address-increment, which allows to write a sequence of registers as long as CS remains in active state.

8.5.1.3 Frame Read (FR)

“Frame Read” (FR) allows a sequential and repeated read-out of up to 4 pre-configured register address values comprising a frame:

1. {1’b0, SPI_FADDR0 [7:0], 1’b0} : default pointing to register SC_FC1 [15:0]
2. {1’b0, SPI_FADDR1 [7:0], 1’b0} : default pointing to register SC_FC2 [15:0]
3. {1’b0, SPI_FADDR2 [7:0], 1’b0} : default pointing to 0x00 (not transmitted)
4. {1’b0, SPI_FADDR3 [7:0], 1’b0} : default pointing to 0x00 (not transmitted)

If SPI_FADDR0 [7:0] = 0, register SC_FC1 [15:0] is transferred (DSP Fast Channel 1). If SPI_FADDR1 or SPI_FADDR2 or SPI_FADDR2 are set to 0, the corresponding values are skipped.

A frame start-byte (FS) can be prepended to each frame when configured with SPI_FRFSEN = 1. The FS is composed of a 4-bit programmable frame start pattern SPI_FRFS [3:0] and a 4-bit rolling counter, which is incremented per frame:

FS [7:0] = { SPI_FRFS [3:0], RC [3:0] }

Each frame can be protected by a CRC-8 sequence when configured with SPI_FRCRCEN = 1. The frame check sequence of type CRC-8-CCITT includes all data value and the optional frame start byte with the generator polynomial:

$$x^8 + x^2 + x + 1$$

With SPI_DMY [1] = 1 an additional delay byte can be introduced before the first data frame which allows adjusting the word alignment of the data transfer.

SPI_FRINV [3:0] allows to binary invert the transferred data words of FADDR0 ... FADDR3 by setting the corresponding bit. This can be used as an alternative data protection method in conjunction with repetitive data transfer.

In FR mode the transmission of frames is continued as long as CS remains in active state.

Fast channel data (SC_FC1, SC_FC2) is captured from the DSP at the beginning of each frame before the DATA (FADRR0) [15:8] byte, see Figure 25.

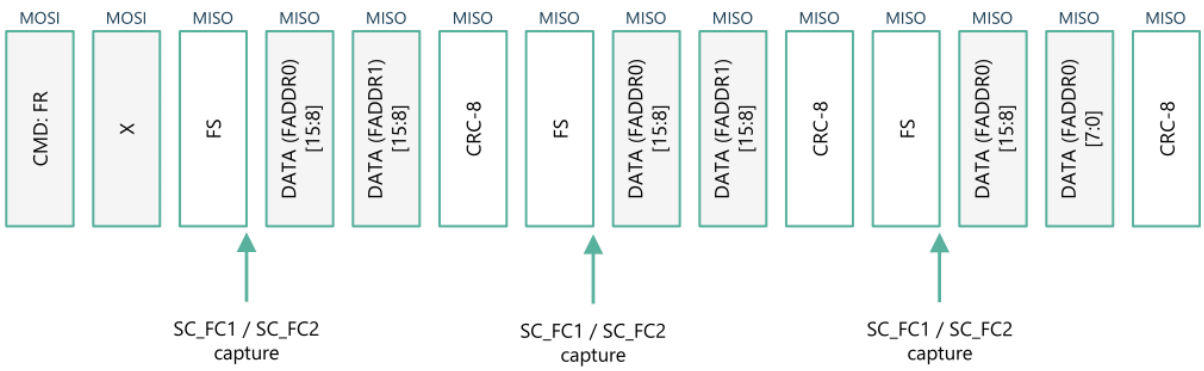


Figure 25: DSP Fast Channel data capture points for FR with 2-byte DATA + FS + CRC-8

The DSP capturing lead time can be controlled to (SPI_CPTLT [2:0] + 1) / f_{SCLK} before SCLK sampling edge of the DATA(FADDR0) [15] (MSB). Both fast channels are synchronously sampled. For f_{SCLK} > 2 MHz, SPI_CPTLT must be ≥ 1 to not violate the bus access duration SPI_t_{BUS}, refer to Section 8.5.2.

Other DMA registers are captured with a lead time of ($8/f_{SCLK} - 2/f_{AC}$) before the SCLK sampling edge of DATA(FADDRx) [15].

8.5.1.4 Super Frame Read (SFR)

The command code 6'b110100 initiates a Super Frame Read (SFR) transaction, which allows the synchronous Fast Channel data capture and sequential TDMA transmission with multiple SPI slaves sharing the same MISO bus. Figure 26 shows an example of a configuration with 2 devices, with a FR configuration with only FS + DATA (FADDR0) + CRC-8, e.g. to transfer the DSP fast channel SC_FC1.

A super frame is configured by its frame length in bytes SPI_SFRL [7:0], which defines the period after which each slave repeats capturing data and transmitting this data in a single FR frame. SPI_SFRL should be configured equal for all participating SPI SFR slaves and needs to be greater than the sum of all FR frames lengths from these slaves.

SPI_SFRDLY [7:0] allows to configure the individual transmission delay in bytes per SPI SFR slave. After start of the super frame each device will keep signal MISO in Hi-Z for SPI_SFRDLY · 8 SCLK cycles before starting a transmission of the individual FR configuration.

As shown in Figure 26, the SPI_SFR_SCPT bit gives 2 options for the capturing of the Fast Channel DSP data into the SFR frames.

SPI_SFR_SCPT	DSP Fast Channel capture timing
0 (default)	Each slave captures at (SPI_CPTLT [2:0] + 1) / f_{SCLK} before SCLK sampling edge of the DATA(FADDR0) [15] of their FR response
1	All slaves capture at (SPI_CPTLT [2:0] + 1) / f_{SCLK} before SCLK sampling edge of the DATA(FADDR0) [15] as for SPI_SFRDLY = 0

Table 54: SPI super frame capture timing

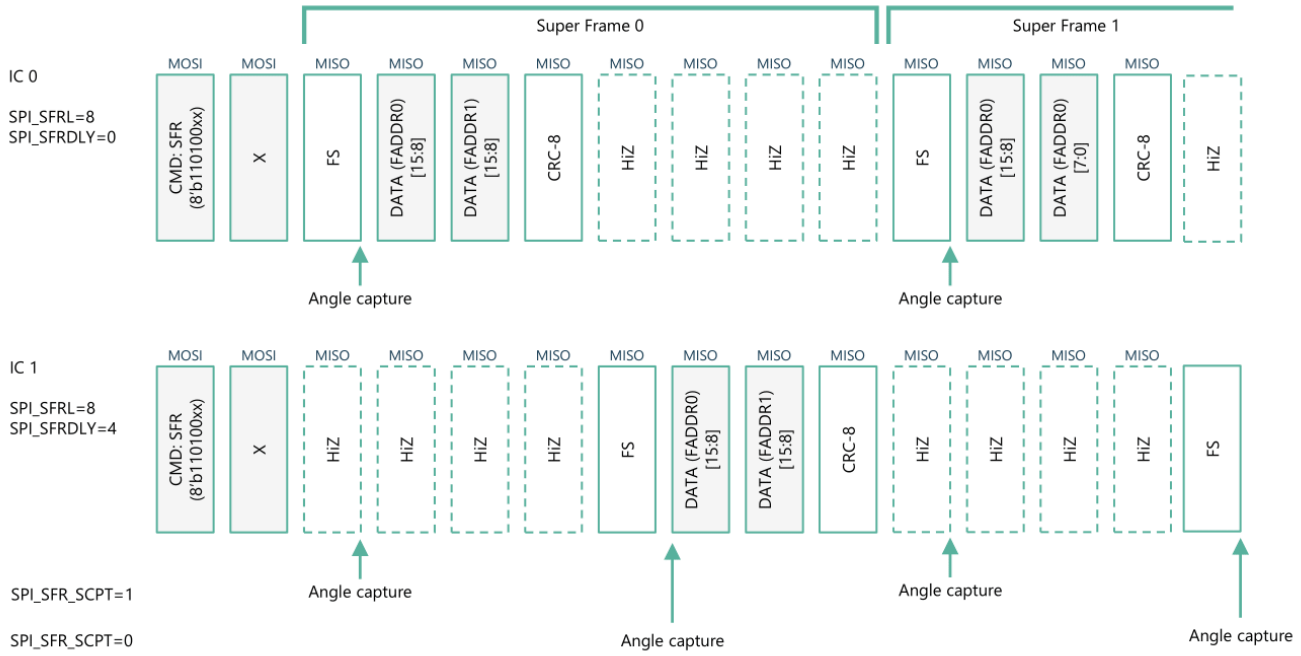


Figure 26: Super Frame configuration with 2 SPI slave devices on shared MISO bus

8.5.2 SPI timing characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SPI clock frequency	f_{SCLK}	0.04		10	MHz	EMC filter off, $f_{AC} > f_{SCLK}/2$
SPI CS active until SCLK active edge delay	SPI_t_{CS0}	0.5			$1/f_{SCLK}$	PROTOCOL = SPI, SPI_DBNC = 0, SPI_DBNC_CS = 0
		250			ns	PROTOCOL ≠ SPI, SPI_DBNC = 0, SPI_DBNC_CS = 0

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SPI inactive delay after SCLK active edge	SPI_t_{CS1}	4			$1/f_{AC}$	SPI WR
		1			$1/f_{SCLK}$	SPI RD, FR, SFR
SPI idle time	SPI_t_{IDLE}	1			$1/f_{SCLK}$	
SPI MISO enable delay after CMD byte	SPI_t_{OE}			200	ns	SPI_DBNC = 0, CMD OK
SPI MISO disable delay after CS inactive	SPI_t_{OD}			200	ns	SPI_DBNC = 0
SPI MISO data delay	SPI_t_{SDO}			40	ns	$C_L \leq 20$ pF
SPI bus access duration	SPI_t_{BUS}			4	$1/f_{AC}$	

Table 55: SPI timing parameters

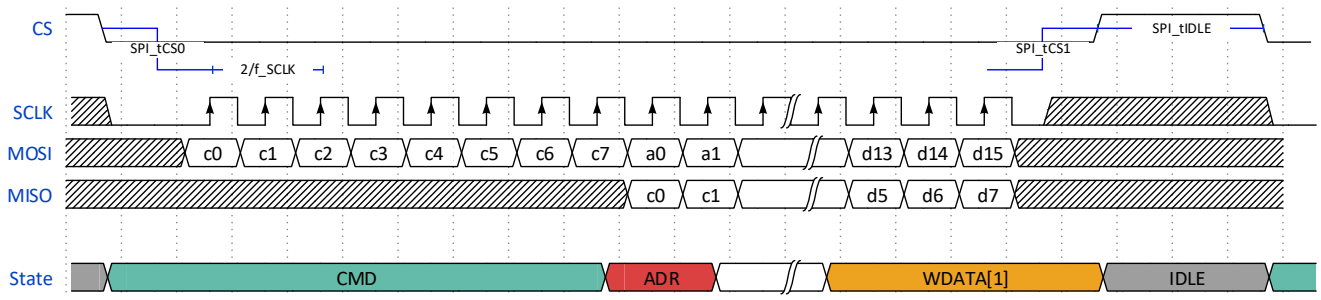


Figure 27: SPI timing example for SPI_WR

The SPI offers digital debouncing for the signals MOSI, SCLK and CS, which can be controlled with fields SPI_DBNC [3:0] and SPI_DBNC_CS [3:0] respectively. This debouncing creates following delays:

- τ_{SCLK} (SPI_DBNC) = τ_{MOSI} (SPI_DBNC) = SPI_DBNC / f_{RCO}
- τ_{CS} (SPI_DBNC_CS) = 2·SPI_DBNC / f_{RCO}

These delays lead to a limitation of the SPI clock frequency: $f_{SCLK} < 0.4$ / (SPI_t_{SDO} + (SPI_DBNC+1)/f_{RCO}). Also, SPI_t_{CS0} is influenced:

- if SPI_DBNC_CS > 0: SPI_t_{CS0} > (2·SPI_DBNC_CS+1) / f_{RCO}
- if SPI_DBNC > 0: SPI_t_{CS0} > (SPI_DBNC+1) / f_{RCO}

9 Identification items

To ensure traceability and unique identification of the individual parts, the EEPROM stores read-only identifiers for the wafer fab (D_FAB_ID [3:0]), for the wafer lot (D_LOT_ID_HI [5:0], D_LOT_ID_LO [10:0]), for the wafer number within the lot (D_WFR_ID [4:0]), and the X and Y coordinates of the chip within the wafer(D_X_POS_ID [7:0] and D_Y_POS_ID [7:0], respectively), see Section 11.

Additionally, the user disposes of six fields that are freely programmable to arbitrary values: USER_ID0 [7:0] … USER_ID5 [7:0].

10 Functional Safety

According to ISO26262, the MLX90514 achieves ASIL-C. The technical safety concept is described in the Safety Manual. In case of random internal failure detection, the MLX90514 transitions to one of its safe states: it either set its output pin OUT and MISO in a high impedance state (Hi-Z) or indicates safe state trough the output-protocol specific fault reporting, as long as the failure is detected.

10.1 Safety Manual

The Safety Manual, available upon request, contains the necessary information to integrate the MLX90514 component in a safety related item, as Safety Element Out-of-Context (SEooC).

In particular, it includes:

1) The description of the Product Development lifecycle tailored for the Safety Element
2) The top technical safety requirements
3) An extract of the Technical Safety concept
4) The description of Assumptions-of-Use (AoU) of the element with respect to its intended use, including:
   - assumptions on environmental and functional condition
   - assumptions on external safety mechanisms
   - assumptions on end of line calibration
5) The description of safety analysis results at the device level useful for the system integrator; HW architectural metrics and description of dependent failures initiators
6) The description and the result of the functional safety assessment process, the list of confirmation measures and the description of the independency level.

10.2 Safety specification

The top technical safety requirements of the MLX90514 are summarized in Table 56. Please refer to the Safety Manual for more details and boundary conditions. FHTI is given for $f_{AC} = 20\,\text{MHz}$.

Description	Angle error	ASIL	FHTI
The measured electrical angle for channel A and B shall not exceed an error θ_{FS} without safe state indication.	$\theta_{FS} = \pm 3\,°\text{el}$	ASIL C	4 ms
The Vernier angle shall not exceed an error θ_{ver_FS} without safe state indication.	$\theta_{ver\_FS}[°\text{mech}] = \frac{\theta_{FS}}{VDP}$	ASIL C	4 ms
The differential angle shall not exceed an error θ_{diff_FS} without safe state indication.	$\theta_{\text{diff\_FS}}\,[°\text{mech}] = \frac{\theta_{FS} \cdot (N_{\text{MIN}} + N_{\text{SUB}})}{\text{GCD} \cdot N_{\text{MIN}} \cdot N_{\text{SUB}}}$	ASIL C	4 ms

Table 56: Functional safety specification

10.3 Safe States

In all fail-safe states, the sensor application function and the LCO remains active until the fault condition forces an internal halt.

10.3.1 Safe State 2

Safe State 2 (SS2) reports critical faults, which may impact controlled reporting through the output interface. State SS2 has priority over SS3.

In SS2, all output pins OUT and MISO are switched to tri-state (high impedance Hi-Z) for all application output protocols. In conjunction with a pull-up resistor R_{PU} to VS placed at the corresponding ECU inputs, the IC indicates failure-band-high. In conjunction with a pull-down resistor R_{PD} to GND placed at the corresponding ECU inputs, the IC indicates failure-band-low.

Note that in SS2 the SPI programming transactions Register Read and Register Write are still supported as far as possible, while Frame Read and Super Frame Read commands return Hi-Z on pin MISO.

10.3.2 Safe State 3

Safe state 3 (SS3) is the default reporting mode for all faults which do not affect the operation of the output interface. In safe state SS3 the output interface remains active and reports the fault as part of the protocol as follows:

Interface	SS3 reporting
SENT/SPC	• Status bit 0 is set to 1 • FC1 data is set to fault band value SC1_YE [1], e.g. 4089 .. 4095, or 0 as defined in SENT SAE J2716 Section E.1.2. (Reserved signaling ranges) • If SENT_REPORT_MODE_ANA = 1, in H.4 the redundant nibble is inverted • Serial message status is non-zero indicating the fault source, see Section 8.1.7
PWM	• FC1 data is set to fault band value SC1_YE [1]
SPI (FR)	• FC1 data is set to fault band value SC1_YE, else frame start field must be enabled (SPI_FRFSEN = 1) [2] • The frame start field is binary inverted

Table 57: SS3 reporting overview per interface

Note:

[1] The fault band value / duty-cycle for SENT/SPC/PWM is defined by SC1_YE [15:0] (see Section 7.5.10.1). The IC verifies if this value is set outside the signaling band between SC1_Y1 [15:0] and SC1_Y2 [15:0]. If this is violated the device reports safe state SS2.

[2] The fault band value for SPI (FR) is defined by SC1_YE [15:0] (see Section 7.5.10.1). If SC1_YE is configured outside the signaling band between SC1_Y1 [15:0] and SC1_Y2 [15:0], SC1_YE is NOT reported, instead the FC1 data transfer is continued. In this case SPI_FRFSEN = 1 must be configured to enable the frame start field, otherwise the device reports safe state SS2.

Note that transitions to SS3 during SPI frame transmissions can cause CRC-errors for that frame.

10.4 Safety mechanism and monitors

Table 58 depicts the list of built in diagnostics or safety mechanisms. For more details refer to the Safety Manual.

Safety mechanism	Description	Safe state
AFE / Sensor diagnostics		
DIAG_LC_A	LCO amplitude difference monitor	SS3
DIAG_LC_P	LCO period monitor	SS3
DIAG_LC_OC	LCO overcurrent monitor	SS3
DIAG_SSL	Sensor short / loss monitor	SS3
DIAG_TRIA	Tri-Amp monitor	SS3
DIAG_FE	Frontend monitor	SS3
DIAG_AGC	AGC monitor	SS3
DIAG_ADC_LIN	ADC linearity selftest	SS3
Digital-IC Diagnostics		
DIAG_NVM_ECC	EEPROM double-bit error	SS2
DIAG_NVM_SR	EEPROM shadow register monitor	SS2
DIAG_DSP	DSP monitor	SS3
DIAG_ACC	Angular acceleration monitor	SS3
DIAG_SPEED	Angular speed monitor	SS3
DIAG_DRIFTC	Delay compensation monitor	SS3
DIAG_SCXY	Signal conditioning monitor	SS2
DIAG_INTP	Interpolator monitor	SS2
DIAG_SSI[A,B]	Signal strength monitor	SS3
DIAG_DIFF	Difference calculation monitor	SS3
DIAG_VER	Vernier calculation monitor	SS3
DIAG_VRES	Vernier reserve monitor	SS3
ABE / Interface diagnostics + mechanisms		
DIAG_SENT	SENT/SPC controller monitor	SS3
DIAG_PWM	PWM output monitor	SS2
DIAG_PWMRX	PWM RX period monitor	SS3
DIAG_EXT_SENT, DIAG_EXT_SPC	SENT / SPC rolling counter, CRC, redundant nibble and data fault banding	n/a
DIAG_EXT_PWM	PWM data fault banding	n/a

Safety mechanism	Description	Safe state
DIAG_EXT_SPI	SPI rolling counter, CRC, and frame start pattern	n/a
Supply system diagnostics		
DIAG_VS, DIAG_VS_OV_5V	External supply voltage monitors	SS2
DIAG_VAUX, DIAG_VDDA	Analog supply voltage monitors	SS2
DIAG_VDDD	Digital supply voltage monitor	POR
DIAG_BG, DIAG_BIAS	Bandgap, bias, reference monitors	SS2
DIAG_GC	Ground comparator	SS2
DIAG_TEMP	Over-/(Maximum)-/Under-temperature monitor	SS3 / (SS2)
Mechanisms on start-up only		
DIAG_NVM_CRC	EEPROM content CRC	SS2
	Supply system and ground comparator LF checks	SS2
	Sensor monitor LF checks	SS2
	LCO frequency monitor LF check	SS2

Table 58: List of diagnostics

The prefix DIAG_EXT refers to assumed external diagnostics utilizing functional safety features of the MLX90514, e.g. CRC. For details refer to the Safety Manual, see Section 10.1.

10.4.1 Return from Safe State into normal operation

When all safety mechanisms indicate return to operational conditions within the safety goal, the output exits safe state and returns to operating mode. With EEPROM register EH_MIN_SS_PERIOD [2:0], a minimum period for the safe state indication can be programmed to support the detection of a safe state in the ECU.

$$min(T_{SS}) = \begin{cases} 2^{9+EH\_MIN\_SS\_PERIOD}/f_{AC} & \text{if EH\_MIN\_SS\_PERIOD > 0} \\ 0 & \text{else} \end{cases}$$

Note that EH_MIN_SS_PERIOD does not only apply to transitions from safe state to normal operating mode, but also to transitions from any safe state into another safe state.

11 Description of memory and registers

11.1 EEPROM

The EEPROM (non-volatile memory) allows accessing the device configurations and calibration values. Both programming and register reading, are supported by SPI and via PGI using the PTC-04/PTC-05 programming tool.

Field	Address	Bit	R/W	Default	Description
CIDA	512 (250)	[1:0]	R/W	0	Chip ID for sensor monitor (Channel A). Defines sensor DC operating point
CIDB		[3:2]	R/W	1	Chip ID for sensor monitor (Channel B). Defines sensor DC operating point
Reserved		4	R/W	1	
DIS_PWRDWN		6	R/W	0	Disable power down mode in case of VS overvoltage
CUS_CHIP_ID		[8:7]	R/W	0	Device ID for MUPeT PGI or SPC. IC addressable via MUPeT SAD command
LC_OSC_EN		9	R/W	1	LCO enable
LC_OSC_AMP		10	R/W	0	LCO amplitude: 0: full amplitude; 1: half amplitude
PHASE		[14:11]	R/W	0	LCO phase delay trimming. Can be used to increase the down-converted signal strength. Each LSB corresponds to 4 ns of delay.
SENTPWM_INV		15	R/W	0	Invert binary waveforms for SENT and PWM
ABE_AOUT_MODE	514 (252)	[2:0]	R/W	4	Analog backend output mode, pin OUT: 0: Reserved 1: Digital output with open-drain-NMOS 2: Digital output with open-drain-PMOS 3: Digital output with Push-Pull 4: Digital output with improved emission, 5 V 5: Digital output with improved emission, 3.3 V
ABE_AOUT_SR		3	R/W	1	ABE_AOUT_MODE in [1,2,3]: Slew rate in binary output modes: 0: fast, 1: slow ABE_AOUT_MODE = [4,5]: 1: improved emission > 400 kHz

Field	Address	Bit	R/W	Default	Description
PROTOCOL		[6:4]	R/W	3	Output protocol: 0: SENT; 1: PWM; 3: SPC, 4,5,6: SPI; else: Reserved
DSP_LFC_LO		[10:8]	R/W	1	Lowest loop filter bandwidth
DSP_LFC_HI		[13:11]	R/W	5	Highest loop filter bandwidth
DSP_SROS		14	R/W	2	Step response overshoot
DSP_ACC_DIS		15	R/W	0	Disable acceleration compensation
DC01A	516 (254)	[15:0]	R/W	0	DC offset compensation value for channel D01A
DC12A	518 (256)	[15:0]	R/W	0	DC offset compensation value for channel D12A
DC20A	520 (258)	[15:0]	R/W	0	DC offset compensation value for channel D20A
DC01B	522 (260)	[15:0]	R/W	0	DC offset compensation value for channel D01B
DC12B	524 (262)	[15:0]	R/W	0	DC offset compensation value for channel D12B
DC20B	526 (264)	[15:0]	R/W	0	DC offset compensation value for channel D20B
EH_MIN_SS_PERIOD	528 (266)	[2:0]	R/W	0	Minimum period the IC will remain in safe state If > 0, $T = 2^{9+EH\_MIN\_SS\_PERIOD} / f_{AC}$, else 0
PWM_PCNT_ON		[6]	R/W	0	PWM period counter enable without PWM protocol
AGC_GAIN_MAX		[9:7]	R/W	4	AGC: maximum PGA gain setting, range [0..4]
AGC_GAIN_MIN		[12:10]	R/W	0	AGC: minimum PGA gain setting, range [0..4]
AC_SEL		[15:13]	R/W	0	Application clock frequency: 3: 10 MHz; 5: 5 MHz; 6: reserved; else 20 MHz
LINA_GAIN	530 (268)	[2:0]	R/W	0	Angular linearization gain, channel A. If > 0, angle A offset [LSB16] at $4096 \cdot xy = signed(LINAxy) \cdot 2^{LINA\_GAIN-1}$, else 0

Field	Address	Bit	R/W	Default	Description
LINB_GAIN		[5:3]	R/W	0	Angular linearization gain, channel B. If > 0, angle B offset [LSB16] at $4096 \cdot xy = signed(LINxy) \cdot 2^{LINB\_GAIN-1}$, else 0
LINA00	532 (270)	[7:0]	R/W	0	Linearization value sensor A at 0/16 * 360 °el
LINA01		[15:8]	R/W	0	Linearization value sensor A at 1/16 * 360 °el
LINA02	534 (272)	[7:0]	R/W	0	Linearization value sensor A at 2/16 * 360 °el
LINA03		[15:8]	R/W	0	Linearization value sensor A at 3/16 * 360 °el
LINA04	536 (274)	[7:0]	R/W	0	Linearization value sensor A at 4/16 * 360 °el
LINA05		[15:8]	R/W	0	Linearization value sensor A at 5/16 * 360 °el
LINA06	538 (276)	[7:0]	R/W	0	Linearization value sensor A at 6/16 * 360 °el
LINA07		[15:8]	R/W	0	Linearization value sensor A at 7/16 * 360 °el
LINA08	540 (278)	[7:0]	R/W	0	Linearization value sensor A at 8/16 * 360 °el
LINA09		[15:8]	R/W	0	Linearization value sensor A at 9/16 * 360 °el
LINA10	542 (280)	[7:0]	R/W	0	Linearization value sensor A at 10/16 * 360 °el
LINA11		[15:8]	R/W	0	Linearization value sensor A at 11/16 * 360 °el
LINA12	544 (282)	[7:0]	R/W	0	Linearization value sensor A at 12/16 * 360 °el
LINA13		[15:8]	R/W	0	Linearization value sensor A at 13/16 * 360 °el
LINA14	546 (284)	[7:0]	R/W	0	Linearization value sensor A at 14/16 * 360 °el
LINA15		[15:8]	R/W	0	Linearization value sensor A at 15/16 * 360 °el
LINB00	548 (286)	[7:0]	R/W	0	Linearization value sensor B at 0/16 * 360 °el

Field	Address	Bit	R/W	Default	Description
LINB01		[15:8]	R/W	0	Linearization value sensor B at 1/16 * 360 °el
LINB02	550 (288)	[7:0]	R/W	0	Linearization value sensor B at 2/16 * 360 °el
LINB03		[15:8]	R/W	0	Linearization value sensor B at 3/16 * 360 °el
LINB04	552 (290)	[7:0]	R/W	0	Linearization value sensor B at 4/16 * 360 °el
LINB05		[15:8]	R/W	0	Linearization value sensor B at 5/16 * 360 °el
LINB06	554 (292)	[7:0]	R/W	0	Linearization value sensor B at 6/16 * 360 °el
LINB07		[15:8]	R/W	0	Linearization value sensor B at 7/16 * 360 °el
LINB08	556 (294)	[7:0]	R/W	0	Linearization value sensor B at 8/16 * 360 °el
LINB09		[15:8]	R/W	0	Linearization value sensor B at 9/16 * 360 °el
LINB10	558 (296)	[7:0]	R/W	0	Linearization value sensor B at 10/16 * 360 °el
LINB11		[15:8]	R/W	0	Linearization value sensor B at 11/16 * 360 °el
LINB12	560 (298)	[7:0]	R/W	0	Linearization value sensor B at 12/16 * 360 °el
LINB13		[15:8]	R/W	0	Linearization value sensor B at 13/16 * 360 °el
LINB14	562 (300)	[7:0]	R/W	0	Linearization value sensor B at 14/16 * 360 °el
LINB15		[15:8]	R/W	0	Linearization value sensor B at 15/16 * 360 °el
DELAY_ANA	564 (302)	[7:0]	R/W	18	Analog processing delay in steps of $26/8/f_{RCO}$ To disable delay compensation set to 0.
DELAY_DIG	566 (304)	[7:0]	R/W	130	Digital processing delay To disable delay compensation set to 0.
DELAY_PS		[15:8]	R/W	25	Digital processing delay for SENT/SPC/PWM pulse shaping (ABE_AOUT_MODE = 4,5), To disable delay compensation set to 0.

Field	Address	Bit	R/W	Default	Description
PHASE_OFS_A	568 (306)	[15:0]	R/W	0	Phase/Angle offset sensor A before signal conditioning, resolution 360/2^16 °el (signed 2's-complement)
PHASE_OFS_B	570 (308)	[15:0]	R/W	0	Phase/Angle offset sensor B before signal conditioning, resolution 360/2^16 °el (signed 2's-complement)
PHASE_OFS_C	572 (310)	[15:0]	R/W	0	Phase/Angle offset channel C before signal conditioning, resolution 360/2^16 °el (signed 2's-complement)
DIFF_CFG	574 (312)	[2:0]	R/W	0	Difference angle input selection: 0: A-B, 1: A-C, 2, 3: B-C, 4: B-A, 5: C-A, 6, 7: C-B
DIFF_N_MIN		[8:3]	R/W	1	Periodicity of minuend
DIFF_N_SUB		[14:9]	R/W	1	Periodicity of subtrahend
DIFF_CS		[15]	R/W	0	CBD reference selection: 0: subtrahend of DIFF 1: minuend of DIFF
VER_CFG	576 (314)	[2:0]	R/W	0	Vernier angle input selection (PA, SA): 0: (A, B), 1: (B, A), 2: (CBD, C), 3: (C, CBD), 4: (A, C), 5: (C, A), 6: (B, C), 7: (C, B)
VER_VDP		[8:3]	R/W	2	Vernier divider primary (PA)
VER_VDS		[14:9]	R/W	1	Vernier divider secondary (SA)
Reserved		15	R/W	0	
VER_VM	578 (316)	[5:0]	R/W	1	Vernier multiplier
DIAG_VER_THD		[9:6]	R/W	4	Vernier calculation diagnostic threshold
DIAG_VRES_THD	580 (318)	[7:0]	R/W	255	Vernier reserve diagnostic threshold
DIAG_DIFF_THD		[15:8]	R/W	4	Difference calculation diagnostic threshold
SC1_X1	582 (320)	[15:0]	R/W	0	Signal conditioning FC1: X1, input range low
SC1_X2	584 (322)	[15:0]	R/W	0	Signal conditioning FC1: X2, input range high
SC1_Y1	586 (324)	[15:0]	R/W	1	Signal conditioning FC1: Y1, output range low
SC1_Y2	588 (326)	[15:0]	R/W	4088	Signal conditioning FC1: Y2, output range high

Field	Address	Bit	R/W	Default	Description
SC2_X1	590 (328)	[15:0]	R/W	0	Signal conditioning FC2: X1, input range low
SC2_X2	592 (330)	[15:0]	R/W	0	Signal conditioning FC2: X2, input range high
SC2_Y1	594 (332)	[15:0]	R/W	1	Signal conditioning FC2: Y1, output range low
SC2_Y2	596 (334)	[15:0]	R/W	4088	Signal conditioning FC2: Y2, output range high
SC1_HL	598 (336)	[7:0]	R/W	128	Signal conditioning FC1: Transition point for clamping high to clamping low as offset from center point of X range; resolution $360°/2^8$
SC2_HL		[15:8]	R/W	128	Signal conditioning FC2: Transition point for clamping high to clamping low as offset from center point of X range; resolution $360°/2^8$
SC1_YE	600 (338)	[15:0]	R/W	4090	Signal conditioning FC1: Fault band value in SS3 If min(SC1_Y1,SC1_Y2) <= SC1_YE <= max (SC1_Y1,SC1_Y2) SS3 changes to SS2 (Hi-Z), except for SPI FR
T_FRAME	602 (340)	[15:0]	R/W	20480	Frame period: SENT: If > 0 frame length [ticks] = T_FRAME [11:0] + 1 PWM: PWM period [$1/f_{AC}$]
USER_ID0	604	[7:0]	R/W	0	Reserved for customer
USER_ID1		[15:8]	R/W	0	Reserved for customer
USER_ID2	606	[7:0]	R/W	0	Reserved for customer
USER_ID3		[15:8]	R/W	0	Reserved for customer
USER_ID4	608	[7:0]	R/W	0	Reserved for customer
USER_ID5		[15:8]	R/W	0	Reserved for customer

Field	Address	Bit	R/W	Default	Description
SPC_FORMAT	610 (342)	[3:0]	R/W	8	SPC frame format: 0: data + checksum 1: data + RC + checksum 2: data + inverted_nibble + checksum 3: data + RC + inverted_nibble + checksum 4: data + temp + checksum 5: data + temp + RC + checksum 6: data + temp + inverted_nibble + checksum 7: data + temp + RC + inverted_nibble + checksum 8: frame configuration set according to SENT_FC_FORMAT
SPC_MEAS_ID		[6:5]	R/W	0	SPC master pulse ID to trigger angle capture
SPC_ TRIGGER_MODE		[8:7]	R/W	1	SPC trigger pulse mode: 0: Synchronous point-to-point 1: Bus mode w/ constant length trigger pulse 2: Bus mode w/ variable length trigger pulse 3: Bus mode w/ fully overlapping trigger pulse
SPC_CSUM_CFG		[10:9]	R/W	0	Fast-channel checksum calculation method: 0,1: checksum i.a.w. SAE J2716 2: Method ”O” i.a.w. SPC2014 3: Method ”E” i.a.w. SPC2014
SPC_CSUM_MODE		[12:11]	R/W	0	Checksum nibble calculation mode in SPC: 0: checksum only 1: checksum + ID 2: checksum + RC 3: checksum + ID + RC
SPC_SCN_BIT_ORDER		[13]	R/W	1	Bit order in Status & Communication Nibble including chip ID and Status bit 0: SENT flavor 1: SPC flavor Note: used only SPC mode, if ID_IN_STATUS=1
SPC_OUT_ON_DLY	612 (344)	[6:0]	R/W	2	Lead time [ticks] between of OUT driver switching Hi-Z -> TX and the SPC sync pulse falling edge. If 0, the transition is at frame start (sync pulse falling edge).

Field	Address	Bit	R/W	Default	Description
SPC_OUT_OFF_DLY		[15:7]	R/W	0	Delay [ticks] between frame start (sync pulse falling edge) and OUT driver switching TX -> Hi-Z. If 0, the transition is at end of pause pulse. SPC_OUT_OFF_DLY must be <= T_FRAME
SPC_TRIGLL_OFS0	614 (346)	[3:0]	R/W	0	Offset for lower detection limit of trigger pulse for ID0
SPC_TRIGLL_OFS1		[7:4]	R/W	0	Offset for lower detection limit of trigger pulse for ID1
SPC_TRIGLL_OFS2		[11:8]	R/W	0	Offset for lower detection limit of trigger pulse for ID2
SPC_TRIGLL_OFS3		[15:12]	R/W	0	Offset for lower detection limit of trigger pulse for ID3
SPC_BLANK_TIME	616 (348)	[8:0]	R/W	5	Blank period [ticks] for which master pulse detection is disabled after unsuccessful trial
SPC_TRG_TIME		[15:9]	R/W	0	If > 0 the total SPC trigger time is set to SPC_TRG_TIME ticks overriding the trigger pulse length settings by SPC_TRIGGER_MODE
SENT_FC_FORMAT	618 (350)	[2:0]	R/W	0	SENT format option 0,1: format H.1 2: format H.2 3: format H.3 4: format H.4 5: format H.5 6: format H.6 7: format H.7
SENT_ SLOW_EXTENDED		5	R/W	1	SENT/SPC serial message definition 0: normal SENT slow message 1: extended SENT slow message (default)
SENT_INIT_GM		6	R/W	0	SENT / SPC initialization frame fast channel 1 definition 0: Initialization frame FC1 = 0 (SENT compliant); In SPC mode only transmitted in case if SS3 1: Initialization frame FC1 = SC1_YE.

Field	Address	Bit	R/W	Default	Description
SENT_TICK_TIME		[9:7]	R/W	4	SENT tick duration: 0: 0.5 µs, 1: 0.75 µs, 2: 1.0 µs, 3:1.5 µs 4: 3.0 µs (normal SENT) else: 6.0 µs (slow SENT) Note, depending on AC_SEL the tick times are rounded to the nearest integer multiple of the application clock period
SENT_SHAPE_CFG		[11:10]	R/W	0	SENT nibble high/low-time configuration: 0: fixed low time (5 ticks); 1: fixed high time (6 ticks); else: 50 % duty cycle Note, only for ABE_AOUT_MODE in [1,2,3]
SENT_SC_FORMAT		12	R/W	1	Slow Channel configuration: 0: short, 1: enhanced serial message
STATUS_IN_CRC		13	R/W	1	1: Status and serial comm. nibble are included in the Fast Channel CRC; 0: not included
ID_IN_STATUS		14	R/W	0	SENT status & communication nibble definition 0: the two slow-message bits i.a.w. SAE J2716 1: the two slow-message bits are replaced by the 2-bit chip ID.
SENT_ REPORT_MODE_ANA		15	R/W	0	SENT H.4 encoding in state SS3: 0: Redundant nibble not inverted 1: Redundant nibble inverted
SENT_FC1_CPT_DLY	620 (352)	[6:0]	R/W	0	Capture delay [ticks] for DSP FC1/FC2 data from falling edge of the SYNC pulse or trigger pulse (SPC: SENT_FC1_CPT_MST)
SENT_FC1_CPT_MST		7	R/W	1	if 1 in SPC mode, data capturing is triggered by falling edge of SPC master pulse, else by falling edge of SYNC pulse (equal to master pulse in SPC fully overlapping mode)
SENT_PS_PWT		[11:8]	R/W	12	Pulse-shaping preamble low time - 3 [ticks]
SENT_RC_INIT		12	R/W	1	Rolling counter (RC) initialization 0: RC stays at 0 during initialization frames 1: RC incrementing during initialization

Field	Address	Bit	R/W	Default	Description
SENT_SC_DIAG_BUF		13	R/W	1	1: diagnostic errors codes are accumulated from last slow channel diagnostic message slot 0: not accumulated
FC1_CFG	622 (354)	[2:0]	R/W	0	Fast Channel 1 data mapping: 0: Angle A 1: Angle B 2: Angle C 3: Difference angle 4: Difference compensated angle else: Vernier angle
FC2_CFG		[5:3]	R/W	1	Fast Channel 2 data mapping for RC[1:0] = 0 0: Angle A 1: Angle B 2: Angle C 3: Difference angle 4: Difference compensated angle 5: Vernier angle 6: SENT/SPC: rolling counter + start pattern, else 0 7: SENT/SPC: Register probe
FC2_CFG_RC1		[8:6]	R/W	0	If > 0: FC2 data mapping for RC[1:0] = 1 Refer to FC2_CFG
FC2_CFG_RC2		[11:9]	R/W	0	If > 0: FC2 data mapping for RC[1:0] = 2 Refer to FC2_CFG
FC2_CFG_RC3		[14:12]	R/W	0	If > 0: FC2 data mapping for RC[1:0] = 3 Refer to FC2_CFG
SENT_FC2_ADR	624 (356)	[7:0]	R/W	39	Address for FC2 register probe; word-aligned
SENT_FC2_OFS0		[11:8]	R/W	0	Bit offset for FC2 register data at even RC
SENT_FC2_OFS1		[15:12]	R/W	0	Bit offset for FC2 register data at odd RC
SENT_SENSOR_TYPE	626	[11:0]	R/W	80	SENT slow message: Sensor type
SENT_REV		[15:12]	R/W	4	SENT slow message: SENT standard revision
SENT_MAN_CODE	628	[11:0]	R/W	6	SENT slow message: Manufacturer code
SENT_SENSOR_ID1	630	[11:0]	R/W	0	SENT slow message: Sensor ID 1
SENT_SENSOR_ID2	632	[11:0]	R/W	0	SENT slow message: Sensor ID 2
SENT_SENSOR_ID3	634	[11:0]	R/W	0	SENT slow message: Sensor ID 3
SENT_SENSOR_ID4	636	[11:0]	R/W	0	SENT slow message: Sensor ID 4

Field	Address	Bit	R/W	Default	Description
SENT_OEM_CODE1	638	[11:0]	R/W	0	SENT slow message: OEM code 1
SENT_OEM_CODE2	640	[11:0]	R/W	0	SENT slow message: OEM code 2
SENT_OEM_CODE3	642	[11:0]	R/W	0	SENT slow message: OEM code 3
SENT_OEM_CODE4	644	[11:0]	R/W	0	SENT slow message: OEM code 4
SENT_OEM_CODE5	646	[11:0]	R/W	0	SENT slow message: OEM code 5
SENT_OEM_CODE6	648	[11:0]	R/W	0	SENT slow message: OEM code 6
SENT_OEM_CODE7	650	[11:0]	R/W	0	SENT slow message: OEM code 7
SENT_OEM_CODE8	652	[11:0]	R/W	0	SENT slow message: OEM code 8
SPI_FADDR0	654 (358)	[7:0]	R/W	0	SPI FR Address 0
SPI_FADDR1		[15:8]	R/W	56	SPI FR Address 1
SPI_FADDR2	656 (360)	[7:0]	R/W	0	SPI FR Address 2
SPI_FADDR3		[15:8]	R/W	0	SPI FR Address 3
SPI_FRFS	658 (362)	[3:0]	R/W	10	SPI FR frame start pattern
SPI_FRFSEN		[4]	R/W	1	SPI FR frame start enable
SPI_FRCRCEN		[5]	R/W	1	SPI FR CRC enable
SPI_FRINV		[9:6]	R/W	0	SPI FR data inversion
SPI_MODE		[11:10]	R/W	0	SPI mode {CPOL, CPHA)}
SPI_DMY		[13:12]	R/W	0	SPI output optional word alignment: [0]: If 1, add DMY byte in SPI RD [1]: If 1, add DMY byte in SPI FR
SPI_SFRL	660 (364)	[7:0]	R/W	0	SPI super frame length [bytes]
SPI_SFRDLY		[15:8]	R/W	0	SPI super frame delay of FR [bytes]
SPI_CPTLT	662 (366)	[2:0]	R/W	1	SPI capture lead time synchronous (SPI_CPTLT + 0.5) / fSCLK before the MSB of byte DATA (FADDR0) [15:8]
SPI_SFR_SCPT		[3]	R/W	0	If 1, synchronize the DSP FC1 / FC2 capture time on all slaves to the position of byte DATA(FADDR0) [15:8] byte as for SPI_SFRDLY = 0
SPI_DBNC_CS		[7:4]	R/W	1	SPI CS debounce filter $\tau_{CS} = SPI\_DBNC\_CS \cdot 2/f_{RCO}$

Field	Address	Bit	R/W	Default	Description
SPI_DBNC		[11:8]	R/W	0	SPI SCLK/MOSI debounce filter $\tau_{CS} = SPI\_DBNC / f_{RCO}$ also applies to INC (PWM input)
Reserved	664 (368)	[4:0]	R/W	0	
Reserved		[15:6]	R/W	2	
PWMRX_X1	666 (370)	[15 :0]	R/W	2048	INC PWM duty cycle range, lower bound
PWMRX_X2	668 (372)	[15 :0]	R/W	63487	INC PWM duty cycle range, upper bound
PWMRX	670 (374)	[0]	R/W	0	INC PWM receiver 1: enable, 0: disable
PWMRX_INV		[1]	R/W	0	INC PWM receiver polarity
PWMRX_DLC		[2]	R/W	1	INC PWM receiver delay compensation 1: enable, 0: disable
DIAG_PWMRX_LO		[9:3]	R/W	63	PWM RX period monitor lower threshold
DIAG_PWMRX_HI	672 (376)	[6:0]	R/W	94	PWM RX period monitor upper threshold
DIAG_PWMRX_EXP		[9:7]	R/W	6	PWM RX period monitor threshold exponent
DIAG_LC_A		[15:10]	R/W	12	LCO differential amplitude monitor threshold
DIAG_LC_P_LO	674 (378)	[7:0]	R/W	60	LCO period monitor, lower limit
DIAG_LC_P_HI		[15:8]	R/W	166	LCO period monitor, upper limit
DIAG_TEMP_THD_LO	676 (380)	[7:0]	R/W	14	Temperature threshold for under-temperature diagnostic: ER_TEMP_LO = 1, if TEMP [11:0] < DIAG_TEMP_THD_LO · 16
DIAG_TEMP_THD_HI		[15:8]	R/W	122	Temperature threshold for over-temperature diagnostic: ER_TEMP_HI = 1, if TEMP [11:0] > DIAG_TEMP_THD_HI · 16
DIAG_ TEMP_THD_MAX	678 (382)	[7:0]	R/W	124	Temperature threshold for over-temperature diagnostic (SS2): ER_TEMP_MAX = 1, if TEMP [11:0] > DIAG_TEMP_THD_MAX · 16
DIAG_ACC_THD		[10:8]	R/W	3	Acceleration monitor threshold

Field	Address	Bit	R/W	Default	Description
PWM_DC_OFS	680 (384)	[8:0]	R/W	0	PWM duty-cycle offset: ΔTPWM_ON = PWM_DC_OFS / fAC [s]
TEMP_CLIP_EN		9	R/W	0	Enable clipping of TEMP [11:0] within [DIAG_TEMP_THR_LO, DIAG_TEMP_THR_HI] · 16
MUPET_CAP		[13:12]	R/W	1	MUPeT PGI cold-activation period: 0: 10 ms; 1, 2: 2.5 ms; 3: cold-activation disabled
TR_VCAP_OCP		[14]	R/W	0	If 1, VCAP current limitation is halved
DE_OV_VSINT		[15]	R/W	0	Disable SS from DIAG_VS_OV_5V (VS OV >6 V)
DIAG_SSIA_LO	682 (386)	[7:0]	R/W	0	Signal strength monitor channel A low limit
DIAG_SSIA_HI		[15:8]	R/W	255	Signal strength monitor channel A high limit
DIAG_SSIB_LO	684 (388)	[7:0]	R/W	0	Signal strength monitor channel B low limit
DIAG_SSIB_HI		[15:8]	R/W	255	Signal strength monitor channel B high limit
DIAG_SPEED_THD_A	686 (390)	[7:0]	R/W	255	Electrical angular speed diagnostic sensor A threshold
DIAG_SPEED_THD_B		[15:8]	R/W	255	Electrical angular speed diagnostic sensor B threshold
DE_TEMPC	688 (392)	[0]	R/W	1	Disable safe state (SS) from DIAG_TEMPC (temperature sensors monitor)
DE_DSP		[1]	R/W	0	Disable SS from DSP diagnostic
DE_DRIFTC		[2]	R/W	0	Disable SS from DIAG_DRIFTC (delay compensation)
DE_VRES		[3]	R/W	1	Disable SS from DIAG_VRES (Vernier reserve)
DE_VER		[4]	R/W	0	Disable SS from DIAG_VER (Vernier calculation)
DE_DIFF		[5]	R/W	0	Disable SS from DIAG_DIFF (difference calculation)
DE_FE		[6]	R/W	0	Disable SS from DIAG_FE (frontend monitor)
DE_TRIA		[7]	R/W	0	Disable SS from DIAG_TRIA (tri-amplifier)
Reserved		[8]	R/W	1	

Field	Address	Bit	R/W	Default	Description
DE_ADC_LIN		[9]	R/W	0	Disable SS from DIAG_ADC_LIN (ADC linearity)
DE_ADC_V8		[10]	R/W	0	Disable SS from DIAG_ADC_LIN (ADC max value)
DE_ADC_0		[11]	R/W	0	Disable SS from DIAG_ADC_LIN (ADC 0 value)
DE_ADC		[12]	R/W	0	Disable SS from DIAG_ADC (ADC internal errors)
DE_AGC		[13]	R/W	0	Disable SS from DIAG_AGC (AGC monitor)
DE_LC_P		[14]	R/W	0	Disable SS from DIAG_LC_P (LCO period)
DE_LC_A		[15]	R/W	0	Disable SS from DIAG_LC_A (LCO amplitude difference)
Reserved	690 (394)	[0]	R/W	0	
DE_SS		[1]	R/W	0	Disable SS from DIAG_SSL (sensor short)
DE_SL		[2]	R/W	0	Disable SS from DIAG_SSL (sensor loss)
DE_SPEED		[3]	R/W	0	Disable SS from DIAG_SPEED (angular speed)
DE_ACC		[4]	R/W	0	Disable SS from DIAG_ACC (acceleration)
DE_BG		[5]	R/W	0	Disable SS from DIAG_BG (bandgap)
DE_VAUX		[6]	R/W	0	Disable SS from DIAG_VAUX (VAUX supply)
DE_VDDA		[7]	R/W	0	Disable SS from DIAG_VDDA (VDDA supply)
DE_OV_VDDD		[8]	R/W	0	Disable SS from DIAG_VDDD (VDDD supply, OV)
Reserved		[9]	R/W	1	
DE_GC		[13:10]	R	0	Disable SS from DIAG_GC Bits 0,1,3: VSSA error Bit 2: VSS error
DE_OV_VS		[14]	R/W	0	Disable SS from DIAG_VS (VS external supply, O V 21 V)
DE_UV_VS		[15]	R/W	0	Disable SS from DIAG_VS (VS external supply, UV)
DE_NVM_SR	692 (396)	[2:0]	R/W	0	If 3, DIAG_NVM_SR is disabled; Else, changes on other shadow registers are corrected by EEPROM content within FDTI
DE_BIAS		[3]	R/W	0	Disable SS from DIAG_BIAS (bias monitor)

Field	Address	Bit	R/W	Default	Description
DE_PWM		[4]	R/W	0	Disable SS from DIAG_PWM (OUT PWM TX)
DE_PWMRX		[5]	R/W	0	Disable SS from DIAG_PWMRX (INC PWM RX)
DE_LC_OC		[6]	R/W	0	Disable SS from DIAG_LC_OC (LCO over current)
DE_TEMP		[7]	R/W	0	Disable SS from DIAG_TEMP (over / under temperature)
DE_TEMP_MAX		[8]	R/W	0	Disable SS from DIAG_TEMP w.r.t DIAG_TEMP_THD_MAX
DE_INTP		[9]	R/W	0	Disable SS from DIAG_INTP (interpolator)
DE_SCXY		[10]	R/W	0	Disable SS from DIAG_SCXY (signal conditioning)
DE_SSI		[11]	R/W	0	Disable SS from DIAG_SSI (signal strength)
Reserved		[12]	R/W	1	
DE_LFSS		[13]	R/W	0	Disable latent fault checks for supply system
DE_LFSM		[14]	R/W	0	Disable latent fault checks for sensor monitor
DE_LFLCO		[15]	R/W	0	Disable latent fault checks for LCO
DE_A	694 (398)	[0]	R/W	0	Disable SS from all diagnostics for channel A
DE_B		[1]	R/W	0	Disable SS from all diagnostics for channel B
DE_SENT		[2]	R/W	0	Disable SS from DIAG_SENT (SENT interface)
EH_WD_EN		[15]	R/W	0	If 1, after boot warm reset is issued after 15 ms in safe state
ANA_VERSION	748	[7:0]	R/W	0xAA	IC version, analog part
DIG_VERSION_L		[15:8]	R/W	0x92	IC version, digital part, low
DIG_VERSION_H	750	[15:0]	R/W	0x161	IC version, digital part, high {DIG_VERSION_H, DIG_VERSION_L} = 24'd90514
D_XPOS_ID	762	[7:0]	R	-	Chip X position
D_YPOS_ID		[15:8]	R	-	Chip Y position
D_WFR_ID	764	[4:0]	R	-	Wafer ID
D_LOT_ID_LO		[15:5]	R	-	Lot ID [10:0]

Field	Address	Bit	R/W	Default	Description
D_LOT_ID_HI	766	[5:0]	R	-	Lot ID [16:11]
D_FAB_ID		[9:6]	R	-	Fab ID

Table 59: EEPROM map

[1] Address between brackets is the shadow register address

11.2 Error Handler

Table 60 lists error handler registers indicating the diagnostic status of the IC.

Field	Address	Bit	R/W	Default	Description
SET_FAULT	48	[1:0]	R/W	0	2: DE_* bits set status of corresponding diagnostic to fault detected: ER_* = 1 else: DE_* disable safe state of diagnostic
ER_TEMPC	50	0	R	0	DIAG_TEMPC error (temperature sensors monitor)
ER_DSP		1	R	0	DSP diagnostic error
ER_DRIFTC		2	R	0	DIAG_DRIFTC (delay compensation) error
ER_VRES		3	R	0	DIAG_VRES (Vernier reserve) error
ER_VER		4	R	0	DIAG_VER (Vernier calculation) error
ER_DIFF		5	R	0	DIAG_DIFF (difference calculation) error
ER_FE_A		6	R	0	DIAG_FE (frontend monitor) channel A error
ER_FE_B		7	R	0	DIAG_FE (frontend monitor) channel B error
ER_TRIA_A		8	R	0	DIAG_TRIA (tri-amplifier) channel A error
ER_TRIA_B		9	R	0	DIAG_TRIA (tri-amplifier) channel B error
ER_ADCA_LIN		10	R	0	DIAG_ADC_LIN (ADC linearity) channel A error
ER_ADCB_LIN		11	R	0	DIAG_ADC_LIN (ADC linearity) channel B error
ER_ADC_V8		12	R	0	DIAG_ADC_LIN (ADC value) error
ER_ADC_0		13	R	0	DIAG_ADC_LIN (ADC 0 value) error
ER_ADC		14	R	0	DIAG_ADC (ADC internal) error
ER_AGC_LO_A		15	R	0	DIAG_AGC (AGC) channel A signal too low error
ER_AGC_LO_B	52	0	R	0	DIAG_AGC (AGC) channel B signal too low error

Field	Address	Bit	R/W	Default	Description
ER_AGC_HI_A		1	R	0	DIAG_AGC (AGC) channel A signal too high error
ER_AGC_HI_B		2	R	0	DIAG_AGC (AGC) channel B signal too high error
ER_LC_P_LO		3	R	0	DIAG_LC_P LCO period too low error
ER_LC_P_HI		4	R	0	DIAG_LC_P LCO period too high error
ER_SS_A		[6:5]	R	0	DIAG_SSL (sensor short) channel A error Bit 0: short to VS or to another sensor with higher VSOP Bit 1: short to GND or to another sensor with lower VSOP
ER_SS_B		[8:7]	R	0	DIAG_SSL (sensor short) channel B error
ER_SL_A		[11:9]	R	0	DIAG_SSL (sensor loss) channel A error Bit 0: IN0 open if ER_SS=0; ignore if ER_SS>0 Bit 1: IN1 open if ER_SS=0; ignore if ER_SS>0 Bit 2: IN2 open if ER_SS=0; ignore if ER_SS>0
ER_SL_B		[14:12]	R	0	DIAG_SSL (sensor loss) channel B error
ER_SPEED_A		15	R	0	DIAG_SPEED (angular speed) channel A error
ER_SPEED_B	54	0	R	0	DIAG_SPEED (angular speed) channel B error
ER_ACC_A		1	R	0	DIAG_ACC (acceleration) channel A error
ER_ACC_B		2	R	0	DIAG_ACC (acceleration) channel B error
ER_SSIA_LO		3	R	0	DIAG_SSI (signal strength) channel A low error
ER_SSIB_LO		4	R	0	DIAG_SSI (signal strength) channel B low error
ER_SSIA_HI		5	R	0	DIAG_SSI (signal strength) channel A high error
ER_SSIB_HI		6	R	0	DIAG_SSI (signal strength) channel B high error
ER_PWMRX		7	R	0	DIAG_PWMRX (INC PWM RX) period error
ER_LC_OC		8	R	0	DIAG_LC_OC (LCO over-current) error
ER_TEMP_LO		9	R	0	DIAG_TEMP (under-temperature) error
ER_TEMP_HI		10	R	0	DIAG_TEMP (over-temperature) error
ER_LC_A		11	R	0	DIAG_LC_A (LCO amplitude difference) error
Reserved		12	R	0	
ER_SENT		13	R	0	DIAG_SENT (SENT interface) error
Reserved		14	R	0	

Field	Address	Bit	R/W	Default	Description
ER_BG		15	R	0	DIAG_BG (bandgap) error
OV_VAUX	56	0	R	0	DIAG_VAUX (VAUX supply) over-voltage error
OV_VDDA		1	R	0	DIAG_VDDA (VDDA supply) over-voltage error
UV_VDDA		2	R	0	DIAG_VDDA (VDDA supply) under-voltage error
OV_VDDD		3	R	0	DIAG_VDDD (VDDD supply) over-voltage error
Reserved		4	R	0	
ER_GC		[8:5]	R	0	DIAG_GC (ground comparator) Bits 0,1,3: VSSA error Bit 2: VSS error
OV_VS		9	R	0	DIAG_VS (VS) over-voltage (>21 V) error
UV_VS		10	R	0	DIAG_VS (VS) unter-voltage error
OV_VSINT		11	R	0	DIAG_VS_OV_5V (VS) over-voltage (>6 V) error
ER_NVM_DED		12	R	0	DIAG_NVM_ECC (EEPROM ECC) double-bit error
ER_NVM_CRC		13	R	0	DIAG_NVM_CRC (EEPROM CRC) error
ER_NVM_SR		14	R	0	DIAG_NVM_SR (EEPROM shadow register) error
ER_BIAS		15	R	0	DIAG_BIAS (bias monitor) error
ER_PWM	58	0	R	0	DIAG_PWM (OUT PWM TX) error
ER_TEMP_MAX		1	R	0	DIAG_TEMP (over-temperature) SS2 error
ER_INTP		2	R	0	DIAG_INTP (interpolator) error
ER_SCXY		3	R	0	DIAG_SCXY (signal conditioning) error
CRC	64	[15:0]	R	0	EEPROM checksum result
STRT_CALC_CRC	66	0	R/W	0	1: Start EEPROM CRC calculation
CRC_CALC_DONE		1	R	0	1: EEPROM CRC updated
Reserved		[15:2]	R	0	
LOCK_KEY	70	[3:0]	R/W	0	Write sequence 0x7, 0x9, 0x4, 0xF to lock EEPROM for programming permanently
Not used		[15:4]	R	0	

Field	Address	Bit	R/W	Default	Description
STATE	72	[7:0]	R	0	Main FSM states: 0x80: EEPROM CRC check 0x01, 0x02, 0x04, 0x20: Initialization 0x08: Normal operation 0x10: SS2 0x40: SS3

Table 60: Error handler register map

11.3 Digital Signal Processing

Table 61 lists the DSP registers including readout of angle and speed and and registers to control the DC offset calibration procedure.

Field	Address	Bit	R/W	Default	Description
AGC_GAIN_A	74	[2:0]	R/W	0	AGC gain value channel A Writable only if AGC_LOCK = 1
AGC_GAIN_B		[5:3]	R/W	0	AGC gain value channel B Writable only if AGC_LOCK = 1
AMP_ADC_A	76	[7:0]	R	0	ADC amplitude channel A as reference for AGC control and DIAG_AGC
AMP_ADC_B		[15:8]	R	0	ADC amplitude channel B as reference for AGC control and DIAG_AGC
TEMP	78	[11:0]	R	0	Temperature value i.a.w. SENT SAE J2716, range [200 : 0.125 : 711.875] [K]
DCCAL_A_REQ	80	0	WO1	0	1: Start signal measurement cycle channel A
DCCAL_B_REQ		1	WO1	0	1: Start signal measurement cycle channel B
DCCAL_DONE		2	R	0	If 1, signal measurement cycle finished, DCCAL_* fields updated
NACC		[5:3]	R/W	0	Averaging period of DC signal measurement cycle $T_{acc} = 2^{NACC+5} \cdot 8/f_{AC}$
AGC_LOCK		6	R/W	0	1: Stop AGC regulation, control gain via AGC_GAIN_A, AGC_GAIN_B Activated by DFT_KEY
Not used		7	R	0	
DCCAL_DC01_HI		[9:8]	R	0	Average 18-bit baseband signal difference of inputs IN0 and IN1 (D01); bits [17:16]

Field	Address	Bit	R/W	Default	Description
DCCAL_DC12_HI		[11:10]	R	0	Average 18-bit baseband signal difference of inputs IN1 and IN2 (D12); bits [17:16]
DCCAL_DC20_HI		[13:12]	R	0	Average 18-bit baseband signal difference of inputs IN2 and IN0 (D20); bits [17:16]
Not used		[15:14]	R	0	
DCCAL_DC01_LO	82	[15:0]	R	0	Average 18-bit baseband signal difference of inputs IN0 and IN1 (D01); bits [15:0] DCCAL_DC* = DCCAL_DC*_HI $\cdot 2^{16}$ + DCCAL_DC*_LO
DCCAL_DC12_LO	84	[15:0]	R	0	Average 18-bit baseband signal difference of inputs IN1 and IN2 (D12); bits [15:0]
DCCAL_DC20_LO	86	[15:0]	R	0	Average 18-bit baseband signal difference of inputs IN2 and IN0 (D20); bits [15:0]
DCCAL_AOSC	88	[15:0]	R	0	Measured average LC oscillator amplitude
LIN_PHASE_A	90	[15:0]	R/W	0	Angular value after linearization channel A Resolution $360°\text{el}/2^{16}$; Writable only if LOCK_PHASE = 1
LIN_PHASE_B	92	[15:0]	R/W	0	Angular value after linearization channel B Resolution $360°\text{el}/2^{16}$; Writable only if LOCK_PHASE = 1
SPEED_LO_A	94	[15:0]	R/W	0	LSB of electrical speed channel A Writable only if LOCK_SPEED = 1
SPEED_LO_B	96	[15:0]	R/W	0	LSB of electrical speed channel B Writable only if LOCK_SPEED = 1
LOCK_SPEED	98	0	R/W	0	1: Lock speed value; disable speed tracking; Activated by DFT_KEY
LOCK_PHASE		1	R/W	0	1: Lock phase value; disable phase tracking Activated by DFT_KEY
DIS_DRIFTC		2	R/W	0	1: Disable delay compensation Activated by DFT_KEY
Not used		[13:3]	R	0	
SPEED_HI_A		14	R/W	0	MSB of electrical speed channel A Writable only if LOCK_SPEED = 1
SPEED_HI_B		15	R/W	0	MSB of electrical speed channel B Writable only if LOCK_SPEED = 1
ACC_A	100	[8:0]	R	0	Angular acceleration offset channel A
ACC_B	102	[8:0]	R	0	Angular acceleration offset channel B

Field	Address	Bit	R/W	Default	Description
Reserved	104	[13:0]	R	0	
FESUMA	106	[7:0]	R	0	Result of sum of differences (D01+D12+D20) channel A
FESUMB		[15:8]	R	0	Result of sum of differences (D01+D12+D20) channel B
SSIA	108	[7:0]	R	0	Signal strength information channel A
SSIB		[15:8]	R	0	Signal strength information channel B
SC_FC1	110	[15:0]	R	0	FC1 value after signal conditioning
SC_FC2	112	[15:0]	R	0	FC2 value after signal conditioning
VRES	114	[15:0]	R	0	Vernier reserve
DFT_KEY	116	[3:0]	R/W	0	10: Enable DSP controls
LC_P_MON_VAL	156	[7:0]	R	0	LCO period measurement value
DIAG_PWM_DC_OFS	158	[8:0]	R	0	PWM duty cycle offset as measured by DIAG_PWM
PWM_PCNT	160	[15:0]	R	0	PWM period counter

Table 61: DSP register map

12 Recommended Application diagrams

In Figure 28 depicts the application diagram for SENT/SPC and PWM output. The ground pins VSS, VSSA and ground connections of other pins and components should be connected by low-impedance vias and interconnects to common system ground plane on the PCB. For embedded applications with SPI please refer to Figure 29.

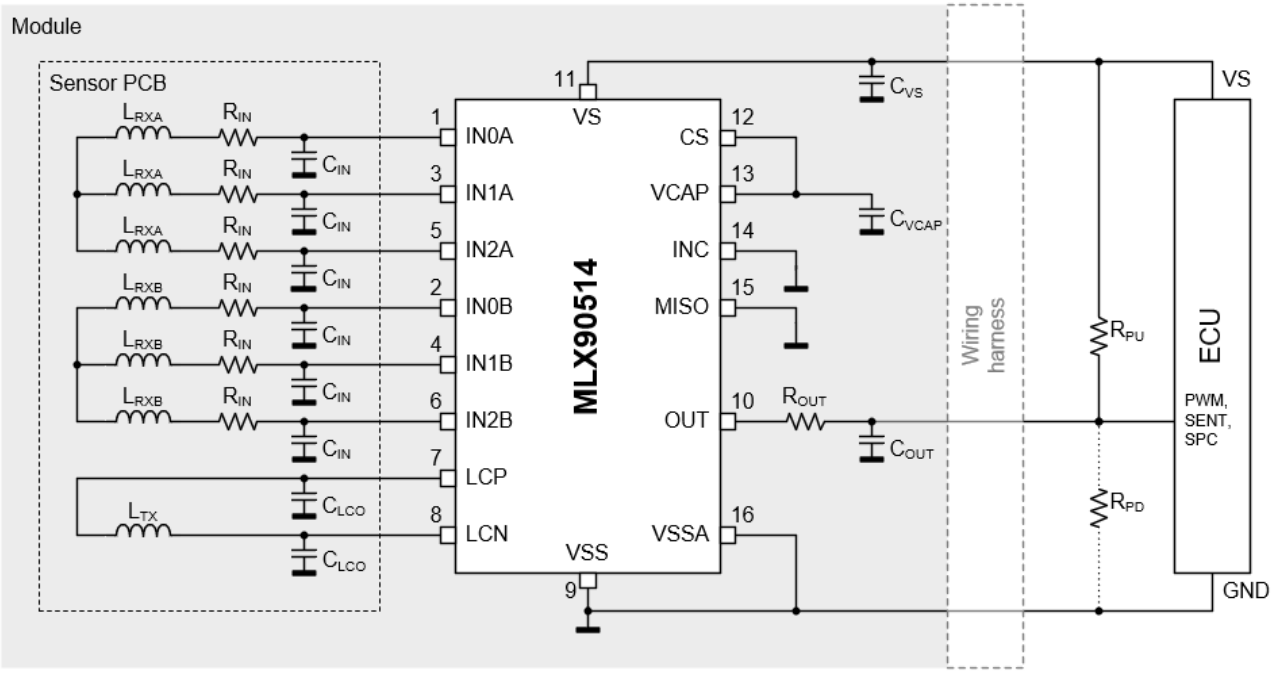


Figure 28: Application schematic for SENT/SPC/PWM

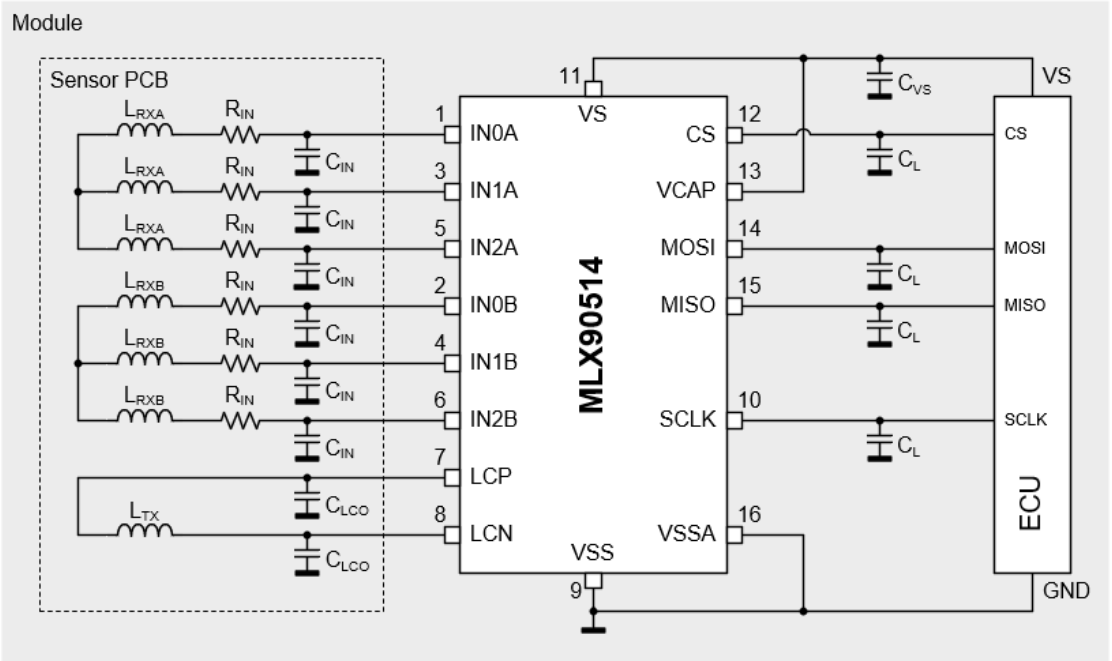


Figure 29: Application schematic for SPI (embedded)

The application circuit components are given in Table 62.

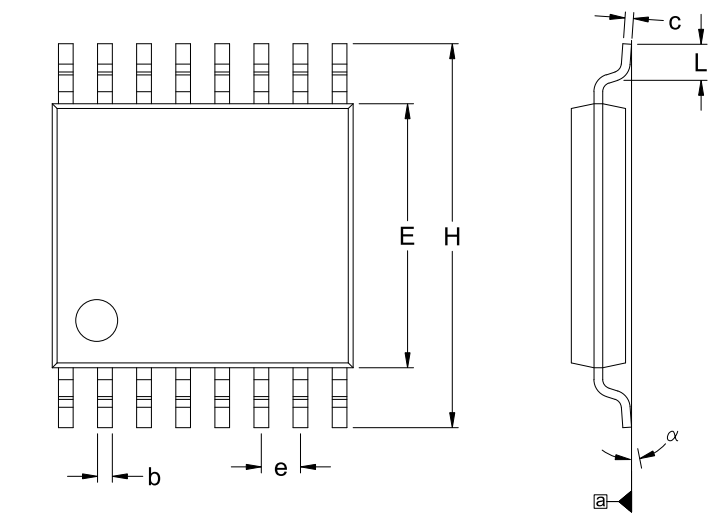
Component	Symbol	Min	Typ	Max	Unit	Comment
Inductor	L_{Tx}	1	4	10	µH	
Inductor	$L_{RxA,B}$	40	200	500	nH	
Resistor	R_{IN}		47		Ω	Optional, EMC related
Capacitor	C_{IN}		100		pF	
Capacitor	C_{LCO}		1.8		nF	
Capacitor	C_{VS}	10	470		nF	
Capacitor	C_{VCAP}	100	470		nF	
Capacitor	C_{OUT}	2.2	4.7	10	nF	SENT, PWM output ABE_AOUT_MODE = 4, T_{tick} = 3 µs. For other tick times C_{OUT} should be proportionally scaled
Capacitor	C_{OUT}	1	2.2	4.7	nF	SENT output ABE_AOUT_MODE = 1, 2, 3 T_{tick} = 1.5 µs, ABE_AOUT_SR = 0
Capacitor	C_{OUT}	2.2	4.7	10	nF	SENT, PWM output ABE_AOUT_MODE = 1, 2, 3 T_{tick} = 3 µs, 6 µs, ABE_AOUT_SR = 0
Capacitor	C_{OUT}	4.7	10	15	nF	SENT, PWM output ABE_AOUT_MODE = 1, 2, 3 T_{tick} = 3 µs, 6 µs, ABE_AOUT_SR = 1
Resistor	R_{OUT}	0	22		Ω	Optional, improves EMC immunity for PWM, SENT, SPC
Output load resistance	R_{PU}/ R_{PD}	3	10	55	kΩ	SENT, PWM output ABE_AOUT_MODE = 4 only
Output load resistance	R_{PU}/ R_{PD}	1.5	10	55	kΩ	SENT, PWM output ABE_AOUT_MODE = 1, 2, 3 In open drain modes the non-driven (pulled) edge timing is determined by the RC time constant of the pull resistor and the load capacitor
Capacitance	C_L			100	pF	Parasitic load in SPI mode

Table 62: Application circuit components

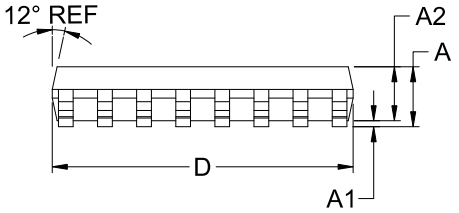
For specific components that are connected to ground with at least one terminal the preferred IC-related ground terminal is listed in above table. However, in general the recommendation is to connect all grounds to a common low impedance ground plane on PCB.

13 Package information

13.1 TSSOP-16 package dimensions



SYMBOL	MINIMUM	MAXIMUM
A	–––	1.10
A1	0.05	0.15
A2	0.85	0.95
D	4.90	5.10
E	4.30	4.50
H	6.40 REF	
L	0.50	0.75
b	0.19	0.30
c	0.09	0.20
e	0.65 BSC	
α	0°	8°



NOTE :

1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS OF MAX 0.15 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTERLEADS FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.08 mm.
5. LEAD TO LEAD COPLANARITY MAX 0.100 MILLIMETERS (mm) WITH RESPECT TO SEATING PLANE a.

Figure 30: TSSOP-16 package dimensions

14 IC handling and assembly

14.1 Storage and handling of plastic encapsulated ICs

Plastic encapsulated ICs shall be stored and handled according to their MSL categorization level (specified in the packing label) as per J-STD-033.

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). The component assembly shall be handled in EPA (Electrostatic Protected Area) as per ANSI S20.20

For more information refer to Melexis Guidelines for storage and handling of plastic encapsulated ICs[1]

14.2 Assembly of encapsulated ICs

For Surface Mounted Devices (SMD, as defined according to JEDEC norms), the only applicable soldering method is reflow.

Melexis products soldering on PCB should be conducted according to the requirements of IPC/JEDEC and J-STD-001. Solder quality acceptance should follow the requirements of IPC-A-610.

Environmental protection of customer assembly with Melexis products for harsh media application, is applicable by means of coating, potting or overmolding considering restrictions listed in the relevant application notes [1]

For other specific process, contact Melexis via www.melexis.com/technical-inquiry

14.3 Environment and sustainability

Melexis is contributing to global environmental conservation by promoting non-hazardous solutions.
For more information on our environmental policy and declarations (RoHS, REACH…) visit

www.melexis.com/environmental-forms-and-declarations

15 Revision history

15/09/2025 (Rev.001)	Product Release

Table 63: Revision history table

[1] www.melexis.com/ic-handling-and-assembly

16 Disclaimer

The content of this document is believed to be correct and accurate. However, the content of this document is furnished "as is" for informational use only and no representation, nor warranty is provided by Melexis about its accuracy, nor about the results of its implementation. Melexis assumes no responsibility or liability for any errors or inaccuracies that may appear in this document. Customer will follow the practices contained in this document under its sole responsibility. This documentation is in fact provided without warranty, term, or condition of any kind, either implied or expressed, including but not limited to warranties of merchantability, satisfactory quality, non-infringement, and fitness for purpose. Melexis, its employees and agents and its affiliates' and their employees and agents will not be responsible for any loss, however arising, from the use of, or reliance on this document. Notwithstanding the foregoing, contractual obligations expressly undertaken in writing by Melexis prevail over this disclaimer.

This document is subject to change without notice, and should not be construed as a commitment by Melexis. Therefore, before placing orders or prior to designing the product into a system, users or any third party should obtain the latest version of the relevant information. Users or any third party must determine the suitability of the product described in this document for its application, including the level of reliability required and determine whether it is fit for a particular purpose.

This document as well as the product here described may be subject to export control regulations. Be aware that export might require a prior authorization from competent authorities. The product is not designed, authorized or warranted to be suitable in applications requiring extended temperature range and/or unusual environmental requirements. High reliability applications, such as medical life-support or life-sustaining equipment or avionics application are specifically excluded by Melexis. The product may not be used for the following applications subject to export control regulations: the development, production, processing, operation, maintenance, storage, recognition or proliferation of:

1. chemical, biological or nuclear weapons, or for the development, production, maintenance or storage of missiles for such weapons;

2. civil firearms, including spare parts or ammunition for such arms;

3. defense related products, or other material for military use or for law enforcement;

4. any applications that, alone or in combination with other goods, substances or organisms could cause serious harm to persons or goods and that can be used as a means of violence in an armed conflict or any similar violent situation.

No license nor any other right or interest is granted to any of Melexis' or third party's intellectual property rights.

If this document is marked "restricted" or with similar words, or if in any case the content of this document is to be reasonably understood as being confidential, the recipient of this document shall not communicate, nor disclose to any third party, any part of the document without Melexis' express written consent. The recipient shall take all necessary measures to apply and preserve the confidential character of the document. In particular, the recipient shall (i) hold document in confidence with at least the same degree of care by which it maintains the confidentiality of its own proprietary and confidential information, but no less than reasonable care; (ii) restrict the disclosure of the document solely to its employees for the purpose for which this document was received, on a strictly need to know basis and providing that such persons to whom the document is disclosed are bound by confidentiality terms substantially similar to those in this disclaimer; (iii) use the document only in connection with the purpose for which this document was received, and reproduce document only to the extent necessary for such purposes; (iv) not use the document for commercial purposes or to the detriment of Melexis or its customers. The confidentiality obligations set forth in this disclaimer will have indefinite duration and in any case they will be effective for no less than 10 years from the receipt of this document.

This disclaimer will be governed by and construed in accordance with Belgian law and any disputes relating to this disclaimer will be subject to the exclusive jurisdiction of the courts of Brussels, Belgium.

The invalidity or ineffectiveness of any of the provisions of this disclaimer does not affect the validity or effectiveness of the other provisions.

The previous versions of this document are repealed.

IATF 16949 and ISO 14001 Certified