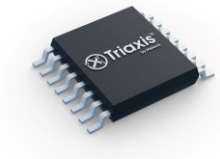
# 1 General description

## 1.1 Features & benefits

- Absolute Angle Position and Speed Tracking up to 200,000 rpm
- On-Chip Signal Processing with Latency Compensation for High-Speed operation and Accurate Absolute Positions Sensing
- 5 V and 3.3 V Application compatible
- Triaxis® Hall Technology
- Programmable Linear Transfer Characteristic with up to 16 points
- Compliant to SIL-2
- JEDEC47L qualified
- Output modes:
  - SPI/SSI/PWM
  - Single-ended and differential ABI/UVW
  - Synchronized readout of multiple devices via SPI
- Packages RoHS compliant
  - Single-Die - QFN-24
  - Dual-Die - TSSOP-16_EP
- 360° stray field immunity up to 4 kA/m


*QFN-24*




*TSSOP-16_EP*

## 1.2 Applications examples

- Absolute Rotary Position Sensor
- Incremental Rotary Position Sensor
- High Speed Encoder
  - Automotive
  - Robotics
  - E-Mobility
  - Industrial Motors
- E-Steering Rotor Position Sensor
- E-Braking Motor Position Sensing

## 1.3 Description

The MLX90382 is a monolithic magnetic position sensor IC that integrates a Triaxis® Hall magnetic front end, an analog-to-digital converter, digital hardware for high-speed signal processing and conditioning, as well as several output drivers.

The MLX90382 is sensitive to three components of the magnetic flux density applied to the IC (i.e. Bx, By, and Bz) and a differential magnetic field in the Z-axis. By programming the sensor, the user can select which axis pair will be used to determine an angle. This flexibility, combined with the appropriate magnetic design, allows the MLX90382 to calculate both the absolute and incremental position of any rotating magnet.

MLX90382 offers five output modes: 1) an industry-standard single-ended and differential ABI interface for incremental angular output, 2) a single-ended and differential UVW signal emulation for BLCD motors, 3) a PWM interface, and 4-5) SPI and SSI interfaces with configurable content that support functional safety requirements. Additionally, the SPI protocol includes a multi-slave synchronized readout capability.

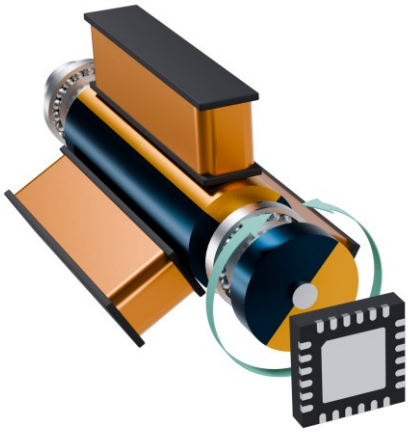


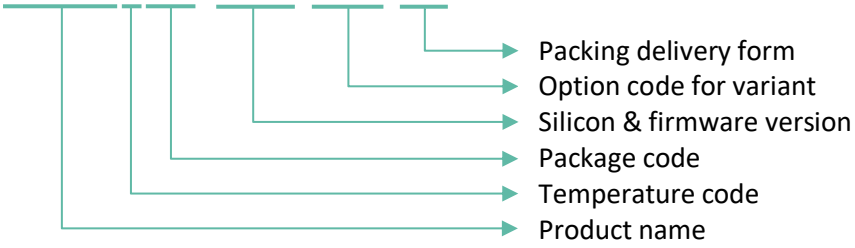
*Figure 1: Application example*

## 2 Ordering information

| Ordering Code | Temperature range (°C) | Package | System Die | Pack-ing | Definition |
|---|---|---|---|---|---|
| MLX90382LLW-ABA-000-RE | -40 to 150 | QFN-24 | Single | Reel | Rotary Mode (Mid-field) On-Axis application |
| MLX90382LLW-ABA-010-RE | -40 to 150 | QFN-24 | Single | Reel | Rotary Mode (Mid-field) Off-Axis application |
| MLX90382LLW-ABA-100-RE | -40 to 150 | QFN-24 | Single | Reel | Rotary Mode (High-field) On-Axis application[1] |
| MLX90382LLW-ABA-600-RE | -40 to 150 | QFN-24 | Single | Reel | Stray Field Immune Rotary Mode |

*Table 1: MLX90382 Ordering Codes*

**MLX90382LLW-ABA-100-RE**




| | |
|---|---|
| Temperature Code: | **L**: -40 °C to 150 °C |
| Package Code: | **LW:** QFN-24 package (Single-Die) (see Section 8.1.1)<br>**GO**: TSSOP-16 package (Dual-Die) (see Section 8.1.2) |
| Option Code - Chip revision | **ABA**-100: **Chip Revision**<br>▪ **ABA**: MLX90382 production version |
| Option Code – Application – Magnetic Configuration | ABA-**1**00: **1-Application - Magnetic Configuration**<br>▪ **0:** Rotary Mode for mid-field magnetic range<br>▪ **1:** Rotary Mode for high-field magnetic range<br>▪ **6:** 360 deg Stray Field Immune Rotary Mode |
| Option Code – Application – Sensing Mode | ABA-0**1**0: **1-Application - Sensing Mode**<br>▪ **0:** On-Axis application (see Section 7.2.1)<br>▪ **1:** Off-Axis application (see Section 7.2.2) |
| Packing Form: | **RE**: Tape & Reel<br>▪ 5000 pcs/reel for QFN-24 package (Single-Die), LW code<br>▪ 4500 pcs/reel for TSSOP-16_EP package (Dual-Die), GO code |

*Table 2: Ordering Codes Information*

[1] *For Application Mode X-Y only (see Section 7.2.1)*

# 3 Contents

# 4 Pin description and block diagram

## 4.1 Pin description

### 4.1.1 Pin description for QFN-24 package

For optimal EMC and ESD behaviour, connect the unused pins to VSS, except unused CS shall be set to VDD. The output driver mode of unused output pins must be set to “Hi-Z”. See Section 6.3.2.

| Pin | Name (1) | I/O (2) | Pin function options (configurable by programming) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | A0 | A1 | A2 | A3 | A4 | A5 |
| 1 | N.C. | | | | | | | |
| 2 | VDD3V3 | S | Pin for decoupling capacitor for 5 V configuration<br>To be shorted to VDD for 3.3 V configuration | | | | | |
| 3..7 | N.C. | | | | | | | |
| 8 | IW | O | ABI: I | UVW: W | ABI: I | UVW: W | ABI: I | UVW: W |
| 9 | BV | O | ABI: B | UVW: V | ABI: B | UVW: V | ABI: B | UVW: V |
| 10 | AU | O | ABI: A | UVW: U | ABI: A | UVW: U | ABI: A | UVW: U |
| 11..16 | N.C. | | | | | | | |
| 17 | VDD | S | Supply for 5 V<br>To be shorted to VDD3V3 for 3.3 V configuration | | | | | |
| 18 | N.C. | | | | | | | |
| 19 | GPIO | O | SPI: MISO | | SSI: DATA | | PWM | |
| 20 | CS | I | SPI: Active low SPI chip select | | | | | |
| 21 | AU_N | O | Hi-Z | | | | ABI: A_N | UVW: U_N |
| 22 | SCLK | I | SPI: SCLK | | SSI: SCLK | | ABI: B_N | UVW: V_N |
| 23 | MOSI | I | SPI: MOSI | | | | ABI: I_N | UVW: W_N |
| 24 | VSS | G | Ground | | | | | |

*Table 3: QFN-24 package pinout*

*Note:*
*(1): The postfix _N refers to logical inverted signals*
*(2): [S] Supply, [G] Ground, [I] Input, [O] Output*

### 4.1.2 Pin description for TSSOP-16_EP package

For optimal EMC and ESD behaviour, connect the unused pins to VSS0/VSS1, except unused CS0/CS1 shall be set to VDD0/VDD1. The output driver mode of unused output pin's must be set to "Hi-Z". See Section 6.3.2.

| Pin | Name | I/O (1) | Pin function options (configurable by programming) | | |
|---|---|---|---|---|---|
| | | | A0 | A1 | A2 |
| Die 0 (Bottom die) | | | | | |
| 1 | VDD0 | S | Supply for 5 V<br>To be shorted to VDD3V30 for 3.3 V configuration | | |
| 2 | GPIO0 | O | SPI: MISO0 | SSI: DATA0 | PWM |
| 3 | CS0 | I | SPI: Active low SPI chip select | | |
| 4 | N.C. | | | | |
| 5 | SCLK0 | I | SPI: SCLK0 | SSI: SCLK0 | |
| 6 | MOSI0 | I | SPI: MOSI0 | | |
| 7 | VSS0 | G | Ground | | |
| 8 | VDD3V30 | S | Pin for decoupling capacitor for 5 V configuration<br>To be shorted to VDD0 for 3.3 V configuration | | |
| Die 1 (Top die) | | | | | |
| 9 | VDD1 | S | Supply for 5 V<br>To be shorted to VDD3V31 for 3.3 V configuration | | |
| 10 | GPIO1 | O | SPI: MISO1 | SSI: DATA1 | PWM |
| 11 | CS1 | I | SPI: Active low SPI chip select | | |
| 12 | N.C. | | | | |
| 13 | SCLK1 | I | SPI: SCLK1 | SSI: SCLK1 | |
| 14 | MOSI1 | I | SPI: MOSI1 | | |
| 15 | VSS1 | G | Ground | | |
| 16 | VDD3V31 | S | Pin for decoupling capacitor for 5 V configuration<br>To be shorted to VDD1 for 3.3 V configuration | | |

*Table 4: TSSOP-16_EP package pinout*

*Note:*
*(1): [S] Supply, [G] Ground, [I] Input, [O] Output*

## 4.2 Block diagram

### 4.2.1 MLX90382 QFN-24 (Single-Die)

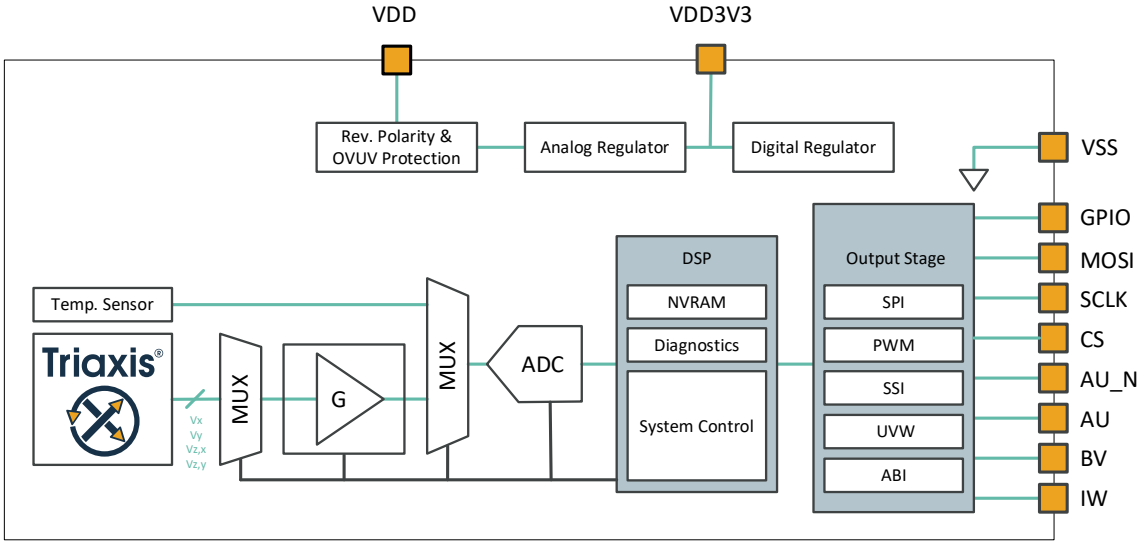



*Figure 2: MLX90382 QFN-24 block diagram*

### 4.2.2 MLX90382 TSSOP-16_EP (Dual-Die)

The isolation resistance between the two dice is specified in Section 5.3.

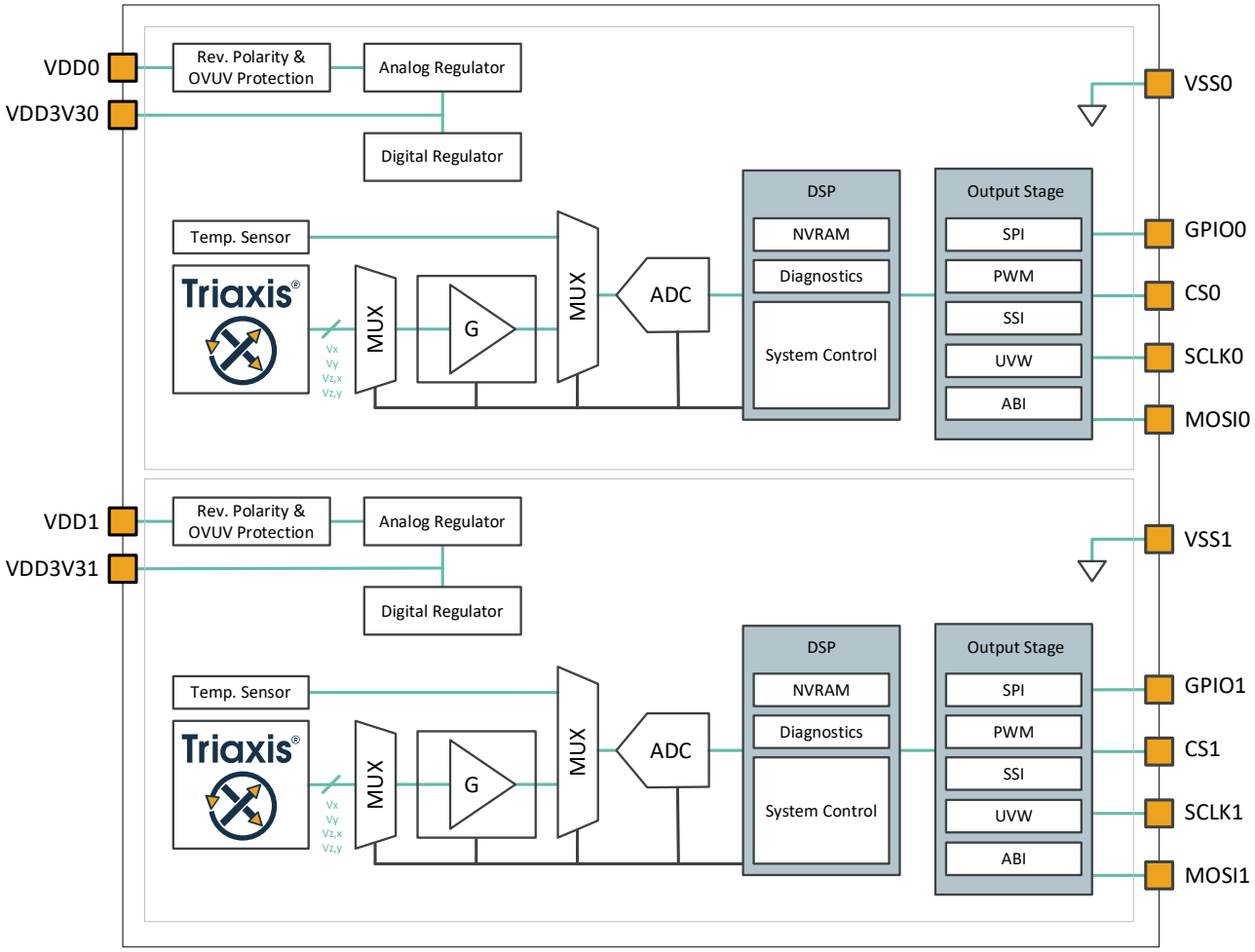



*Figure 3: MLX90382 TSSOP-16_EP block diagram*

# 5 Conditions and specifications

## 5.1 Absolute Maximum Ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions may affect the device reliability.

| Parameter | Symbol | Min. | Max. | Unit | Condition |
|---|---|---|---|---|---|
| Supply Voltage at VDD Pin | $V_{DD}$ | -0.3 | 6.0 | V | |
| Supply Voltage at VDD3V3 Pin | $V_{DD}$ | -0.3 | 4.0 | V | |
| I/O Pin Voltage | $V_{PIN}$ | -0.3 | $V_{DD}$+0.3 | V | |
| ESD CDM Robustness | $V_{CDM}$ | -500 | 500 | V | All pins, except package corner pins, according to JEDEC JS-002 |
| | | -750 | 750 | V | Package corner pins, according to JEDEC JS-002 |
| ESD HBM Robustness | $V_{HBM}$ | -2.0 | 2.0 | kV | |
| Die to Die Voltage | $V_{SS0-SS1}$ | -12.0 | 12.0 | V | VSS0 to VSS1 |
| Operating Temperature | $T_{AMB}$ | -40.0 | 150.0 | °C | |
| Junction Temperature | $T_J$ | | +175 | °C | |
| Storage Temperature | $T_{st}$ | -55 | +170 | °C | |
| Magnetic Flux Density | $B_{max}$ | -1 | 1 | T | |
| NVRAM erase/write cycles | | | 100,000 | Cycles | At 25 °C |

*Table 5: Absolute maximum ratings*

## 5.2 Electrical operating conditions & specifications

### 5.2.1 3.3 V Operating Mode supply

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 3.3 | | V | Pin VDD & VDD3V3 shorted |
| | | -5 | | +5 | % $V_{DD}$ | |
| Supply Current | $I_{DD}$ | | | 10.0 | mA | IMC, excluding output I/F |
| | | | | 11.0 | mA | Stray field immune mode, excluding output I/F |
| Under Voltage Detection Level On | $V_{UVD\_LH\_3V3}$ | 2.7 | 2.825 | 2.95 | V | Supply voltage $V_{DD}$ falling |
| Under Voltage Detection Level Off | $V_{UVD\_HL\_3V3}$ | 2.75 | 2.875 | 3.0 | V | Supply voltage $V_{DD}$ rising |
| Under Voltage detection Hysteresis | $V_{UVD\_Hyst\_3V3}$ | 0.02 | 0.05 | 0.15 | V | |
| Over Voltage Detection Level On | $V_{OVD\_LH\_3V3}$ | 3.6 | 3.75 | 3.9 | V | Supply voltage $V_{DD}$ rising |
| Over Voltage Detection Level Off | $V_{OVD\_HL\_3V3}$ | 3.45 | 3.65 | 3.8 | V | Supply voltage $V_{DD}$ falling |
| Over Voltage Detection Hysteresis | $V_{OVD\_Hyst\_3V3}$ | 0.05 | 0.1 | 0.35 | V | |

*Table 6: Electrical operating conditions in 3.3 V operating mode*

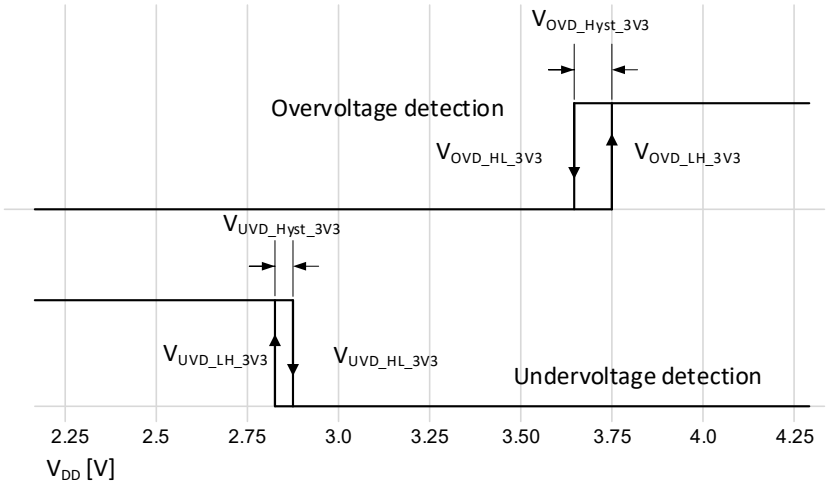



*Figure 4: Over- and under voltage signal detection logic for typical condition in VDD 3.3V mode*

### 5.2.2 5 V Operating Mode

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 5.0 | | V | |
| | | -10 | | +10 | % $V_{DD}$ | |
| Supply Current | $I_{DD}$ | | | 10.0 | mA | IMC, excluding output I/F |
| | | | | 11.0 | mA | Stray field immune mode, excluding output I/F |
| Under Voltage Detection Level Off | $V_{UVD\_HL\_5\ V}$ | 4.1 | 4.25 | 4.4 | V | Supply voltage $V_{DD}$ rising |
| Under Voltage Detection Level On | $V_{UVD\_LH\_5\ V}$ | 3.85 | 4.0 | 4.15 | V | Supply voltage $V_{DD}$ falling |
| Under Voltage Detection Hysteresis | $V_{UVD\_Hyst\_5\ V}$ | 0.1 | 0.25 | 0.4 | V | |
| Over Voltage Detection Level Off | $V_{OVD\_HL\_5\ V}$ | 5.5 | 5.65 | 5.80 | V | Supply voltage $V_{DD}$ falling |
| Over Voltage Detection Level On | $V_{OVD\_LH\_5\ V}$ | 5.75 | 5.9 | 6.0 | V | Supply voltage $V_{DD}$ rising |
| Over Voltage Detection Hysteresis | $V_{OVD\_Hyst\_5\ V}$ | 0.1 | 0.25 | 0.4 | V | |

*Table 7: Electrical operating conditions in 5 V operating mode*

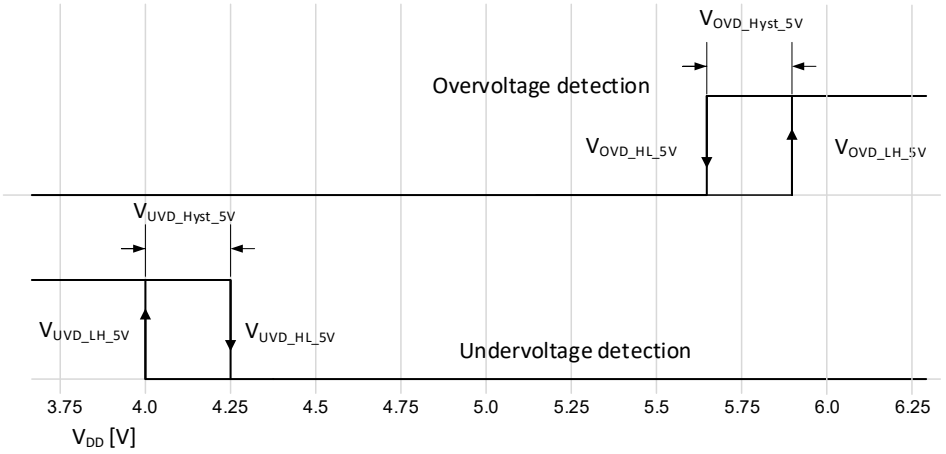



*Figure 5: Over- and under voltage signal detection logic for typical cond. in VDD 5V mode*

## 5.3 Isolation Specification

The specified isolation resistance is only valid for the TSSOP-16_EP package (code GO).

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Die 0 to Die 1 Isolation Leakage Current | $I_{isol}$ | | | 3.0 | µA | Between dice, measured between VSS1 and VSS2 with +/-12 V bias |

*Table 8: Electrical isolation specifications for TSSOP-16_EP*

## 5.4 Thermal Resistance

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Thermal resistance - junction to ambient | $R_{thja}$ | | 28 | | K/W | QFN-24 package with soldered exposed pad |
| | | | 76 | | K/W | QFN-24 package with non-soldered exposed pad |
| | | | 55 | | K/W | TSSOP-16_EP package with soldered exposed pad |
| | | | 107 | | K/W | TSSOP-16_EP package with non-soldered exposed pad |
| Thermal resistance - junction to case | $R_{thjc}$ | | 2 | | K/W | QFN-24 package |
| | | | 31 | | K/W | TSSOP-16_EP package |

*Table 9: Thermal resistance specification (based on simulation)*

## 5.5 Dynamic Operating Specification & Condition

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Rotational Speed (electrical) | $v_{el}$ | -200 | | 200 | krpm | |
| Rotational Acceleration (electrical) | $a_{el}$ | -10000 | | 10000 | krpm/s | Dynamic behaviour see Section 6.2.4. |

*Table 10: Angle operating specification & condition*

## 5.6 Timing specifications

### 5.6.1 General Timing Specifications

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Main Clock Frequency | $f_{RCO}$ | | 20.0 | | MHz | Trimmed. Including thermal and lifetime drift. |
| | | -5 | | 5 | % $f_{RCO}$ | |
| Application Clock Frequency | $f_{AC}$ | | $f_{RCO}$ | | MHz | Trimmed. Including thermal and lifetime drift. |
| Fault Handling Time Interval | FHTI | | | 1.0 | ms | See Section 6.10 |
| System Start-up Time | $T_{Start}$ | | | 1.0 | ms | Adaptive loop filter enabled (see Section 6.2.4) |

*Table 11: General timing specifications*

### 5.6.2 Signal Processing Timing Specification

Unless otherwise specified, the electrical specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Processing Delay | $\tau_P$ | -333.0 | | 333.0 | ns | With delay compensation, excluding output interface. *DSP_DRIFT_DIS[5]* = 0. |
| | | | | 6.0 | µs | No delay compensation, excluding output interface. *DSP_DRIFT_DIS[5]* = 1. |

*Table 12: Signal processing timing specification*

## 5.7 Magnetic Field Specifications

### 5.7.1 Rotary Mode - Mid-Field Variant (Option Code -000 and -010)

Unless otherwise specified, the magnetic field specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Number of Magnetic Poles | $N_P$ | | 2 | | | |
| Magnetic Flux Density Norm (Medium Field IMC) | $B_{NORM}$ | 10.0 | | | mT | $\sqrt{B_x^2 + B_y^2}$ (x-y mode)<br>$\sqrt{B_x^2 + \left(\frac{1}{G_{IMC}} B_z\right)^2}$ (x-z mode)<br>$\sqrt{B_y^2 + \left(\frac{1}{G_{IMC}} B_z\right)^2}$ (y-z mode) |
| Magnetic Flux Density in X-Y plane | $B_X$, $B_Y$ | | | 70.0 | mT | $\sqrt{B_x^2 + B_y^2}$ |
| Magnetic Flux Density in Z direction | $B_Z$ | | | 70.0 | mT | |
| IMC Gain coefficient | $G_{IMC}$ | | 1.15 | | | |

*Table 13: Magnetic field specification for Rotary Mode Mid-Field Variant (Option Code -000 and -010)*

### 5.7.2 Rotary Mode - High-Field Variant (Option Code -100)

Unless otherwise specified, the magnetic field specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Number of Magnetic Poles | $N_P$ | | 2 | | | |
| Magnetic Flux Density (High-Field IMC) | $B_{NORM}$ | 40.0 | | | mT | $\sqrt{{B_x}^2 + {B_y}^2}$ (x-y mode)<br>$\sqrt{{B_x}^2 + \left(\frac{1}{G_{IMC}} B_z\right)^2}$ (x-z mode)<br>$\sqrt{{B_y}^2 + \left(\frac{1}{G_{IMC}} B_z\right)^2}$ (y-z mode) |
| Magnetic Flux Density in X-Y plane | $B_X$, $B_Y$ | | | 120.0 | mT | $\sqrt{{B_x}^2 + {B_y}^2}$ |
| Magnetic Flux Density in Z direction | $B_Z$ | | | 70.0 | mT | TSSOP-16_EP (Package Code: GO) |
| | | | | 85.0 | mT | QFN-24 (Package Code: LW) |
| IMC Gain coefficient | $G_{IMC}$ | | 0.53 | | | |

*Table 14: Magnetic field specification for rotary mode High-Field variant (Option Code -100)*

### 5.7.3 Stray Field Immune Rotary Mode (dBz) (Option Code -600)

Unless otherwise specified, the magnetic field specifications are valid for a temperature range of [-40, 150] °C and specified nominal supply voltage ranges.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Number of Magnetic Poles | $N_P$ | | 2 | | | |
| Magnetic Flux Density Gradient | $\frac{\Delta B_Z}{\Delta XY}$ | 10.0 | | 128.0 | $\frac{\text{mT}}{\text{mm}}$ | $\sqrt{\left(\frac{\Delta B_Z}{\Delta X}\right)^2 + \left(\frac{\Delta B_Z}{\Delta Y}\right)^2}$ ($dB_Z$ mode) |
| Magnetic Flux Density (dBz mode) | Bz | | | 100.0 | mT | |
| Hall Plate Spacing | ΔX, ΔY | | 1.10 | | mm | |

*Table 15: Magnetic field specification for stray field immune rotary mode (Option Code -600)*

### 5.7.4 Constraint on Magnetic Flux Density Slew Rate

The amplitude of the magnetic flux density in all directions may vary over time, primarily due to factors such as temperature variations and mechanical alignment drifts, including the air gap drift between the magnet and the IC. The characteristic of the MLX90382ABA IC limits[2] the rate of change in magnetic flux density in all spatial directions as follows:

$$\frac{\Delta B}{\Delta t} \leq B(t_0) \cdot S_B$$

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Magnetic Flux Density Slew Rate | $S_B$ | | | 5.8 | $\frac{1}{\text{ms}}$ | |

*Table 16: Constraint on Magnetic Flux Density Slew Rate*

[2] *If the specified dB/dt limit does not meet the requirements of your application, please contact Melexis.*

## 5.8 Angular Accuracy specifications

### 5.8.1 Performance Conditions

The MLX90382 accuracy specifications are defined for two different ranges of performance conditions, nominal (see Section 5.8.4) and limited (see Section 5.8.5) performance, which are defined by the ambient temperature and the magnetic flux density/gradient range (see Figure 6).

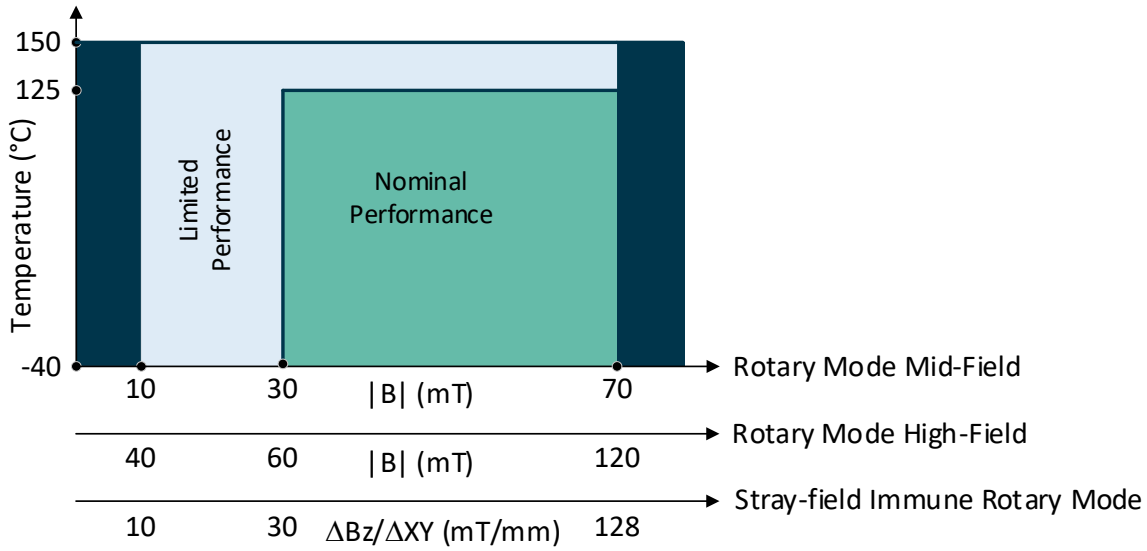



*Figure 6: Performance condition definition for rotary mode with different variants*

### 5.8.2 Definitions

This section defines several parameters, which are used for the magnetic specifications.

#### *5.8.2.1 Intrinsic Linearity Error*

The Intrinsic Linearity Error LE accounts for various error sources within the IC, such as offset, sensitivity mismatch and orthogonality error, assuming an ideal magnetic field. In cases of speed and acceleration, an additional dynamic angular offset ($\theta_{vel,\tau\_P}$) to the Intrinsic Linearity Error is to be expected. When integrated into a sensor module and its associated mechanical and magnetic tolerances, the overall output linearity error increases. The overall linearity error can be reduced through I/Q mismatch calibration (see Section 6.2.5) and 16-point linearization (see Section 6.2.6). Consequently, once properly calibrated, this error is not the critical factor in most applications.

#### *5.8.2.2 Total drift*

After End of Line (EoL) calibration, variation due to temperature and ageing effects are referred to as the total drift $\partial\theta_{TT}$:

$$\partial\theta_{TT} = \max\{\theta(\theta_{IN}, T, t) - \theta(\theta_{IN}, T_{RT}, t_0)\}$$

where $\theta_{IN}$ represents the input angle, $T$ is the operating temperature, $T_{RT}$ is the room temperature, and $t$ is the elapsed time since calibration. $t_0$ represents the start of the sensor's operational life. Note that the total drift $\partial\theta_{TT}$ is always measured relative to the angle at room temperature. In this datasheet, $T_{RT}$ is typically defined at 35 °C, unless stated otherwise. The total drift specification is valid for all angles.

### 5.8.3 General Performance

Unless otherwise specified, valid before EoL calibration and for all applications under the temperature range of [-40, 150] °C.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Dynamic Angular Offset | $\theta_{vel,\tau\_P}$ | -0.1 | | 0.1 | deg | $v_{el}$ = 50 krpm, the value is proportional to the occurring processing delay. $\theta_{Vel,\tau\_p} = 6\ \tau_p\ v_{el.}$ |

*Table 17: General accuracy performance specifications*

### 5.8.4 Nominal Performance

A homogeneous magnetic field is utilized to define magnetic performance specification. The performance may decrease with other magnetic sources.

#### *5.8.4.1 Rotary mode on-axis (Option Code -000 and -100)*

Unless otherwise specified, all values are valid before EoL calibration and for all applications under following nominal performance conditions: Temperature range [-40, 125] °C, $v_{el} \leq$ 50 krpm, Magnetic flux density |B| ≥ 30 mT (IMC-Midfield) and |B| ≥ 60 mT (IMC-Highfield).

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| XY – Intrinsic Linearity Error, IMC | $LE_{\_IMC\_XY}$ | -0.5 | | 0.5 | deg | |
| XZ – Intrinsic Linearity Error, IMC | $LE_{\_IMC\_XZ}$ | -1.0 | | 1.0 | deg | |
| YZ – Intrinsic Linearity Error, IMC | $LE_{\_IMC\_YZ}$ | -1.0 | | 1.0 | deg | |
| XY – Total Drift, IMC | $\partial\theta_{TT\_XY}$ | -0.3 | | 0.3 | deg | $T_{RT}$ = 35 °C |
| XZ, YZ – Total Drift, IMC | $\partial\theta_{TT\_XZ\_YZ}$ | -0.4 | | 0.4 | deg | $T_{RT}$ = 35 °C |
| Magnetic Hysteresis, IMC Midfield | $\theta_{EMH\_IMC\_MF}$ | | | 0.1 | deg | Rotary Mode (Midfield variant) |
| Magnetic Hysteresis, IMC Highfield | $\theta_{EMH\_IMC\_HF}$ | | | 0.1 | deg | Rotary Mode (Highfield variant) |
| Angular noise, RMS | $\theta_{STD}$ | | 0.025 | | deg | *DSP_LFC_HI* = 0 |
| | | | 0.035 | | deg | *DSP_LFC_HI* = 3 |

*Table 18: Accuracy specifications for rotary mode on-axis at nominal performance conditions*

#### *5.8.4.2 Rotary mode off-axis (Option Code -010)*

Unless otherwise specified, all values are valid before EoL calibration and for all applications under following nominal performance conditions: Temperature range [-40, 125] °C, $v_{el} \leq$ 50 krpm, Magnetic flux density |B| ≥ 30 mT.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| XZ – Intrinsic Linearity Error, IMC | $LE_{\_IMC\_XZ}$ | -1.0 | | 1.0 | deg | |
| YZ – Intrinsic Linearity Error, IMC | $LE_{\_IMC\_YZ}$ | -1.0 | | 1.0 | deg | |
| XZ, YZ – Total Drift, IMC | $\partial\theta_{TT\_XZ\_YZ}$ | -0.4 | | 0.4 | deg | $T_{RT}$ = 35 °C |
| Magnetic Hysteresis, IMC Midfield | $\theta_{EMH\_IMC\_MF}$ | | | 0.1 | deg | Rotary Mode (Midfield variant) |
| Angular noise, RMS | $\theta_{STD}$ | | 0.025 | | deg | *DSP_LFC_HI* = 0 |
| | | | 0.035 | | deg | *DSP_LFC_HI* = 3 |

*Table 19: Accuracy specifications for rotary mode off-axis at nominal performance conditions*

#### *5.8.4.3 Stray field immune rotary mode (Option Code -600)*

Unless otherwise specified, all values are valid before EoL calibration and for all applications under the following conditions: Temperature range [-40, 125] °C, $v_{el}$ ≤ 50 krpm, Magnetic flux gradient ΔBz/ΔXY ≥ 30 mT/mm.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| XY – Intrinsic Linearity Error, dBz | $LE_{\_DBZ\_XY}$ | -0.7 | | 0.7 | deg | |
| XY – Total Drift, dBz | $\partial\theta_{TT\_DBZ\_XY}$ | -0.6 | | 0.6 | deg | |
| Stray Field Immunity | $\theta_{SF}$ | -0.15 | | 0.15 | deg | QFN-24 (Package Code: LW) In accordance with ISO11452- 8:2015, at 30 °C with stray field of 4 kA/m from any direction |
| | | -0.25 | | 0.25 | deg | TSSOP-16_EP (Package Code: GO) In accordance with ISO11452- 8:2015, at 30 °C with stray field of 4 kA/m from any direction |
| Angular noise, RMS | $\theta_{STD}$ | | 0.025 | | deg | *DSP_LFC_HI* = 0 |
| | | | 0.050 | | deg | *DSP_LFC_HI* = 3 |

*Table 20: Accuracy specifications for stray field immune mode at nominal performance conditions*

### 5.8.5 Limited Performance

A homogeneous magnetic field is utilized to define magnetic performance specification. The performance may decrease with other magnetic sources.

#### *5.8.5.1 Rotary mode on-axis (Option Code -000 and -100)*

Unless otherwise specified, all values are valid before EoL calibration and for all applications under the following conditions: Temperature range [-40, 150] °C, $v_{el}$ ≤ 50 krpm, Magnetic flux |B| ≥ 10 mT (IMC-Midfield) and |B| ≥ 40 mT (IMC-Highfield).

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| XY - Intrinsic Linearity Error, IMC | $LE_{\_IMC\_XY}$ | -1.0 | | 1.0 | deg | |
| XZ - Intrinsic Linearity Error, IMC | $LE_{\_IMC\_XZ}$ | -2.0 | | 2.0 | deg | |
| YZ - Intrinsic Linearity Error, IMC | $LE_{\_IMC\_YZ}$ | -2.0 | | 2.0 | deg | |
| XY - Total Drift, IMC | $\partial\theta_{TT\_IMC\_XY}$ | -0.8 | | 0.8 | deg | $T_{RT}$ = 35 °C |
| XZ, YZ - Total Drift, IMC | $\partial\theta_{TT\_IMC\_XZ\_YZ}$ | -0.8 | | 0.8 | deg | $T_{RT}$ = 35 °C |
| Magnetic Hysteresis, IMC Midfield | $\theta_{EMH\_IMC\_MF}$ | | | 0.2 | deg | Rotary Mode (Midfield variant) |
| Magnetic Hysteresis, IMC Highfield | $\theta_{EMH\_IMC\_HF}$ | | | 0.2 | deg | Rotary Mode (Highfield variant) |
| Angular noise, RMS | $\theta_{STD}$ | | 0.04 | | deg | *DSP_LFC_HI* = 0 |
| | | | 0.10 | | deg | *DSP_LFC_HI* = 3 |

*Table 21: Accuracy specifications for rotary mode on-axis at limited performance conditions*

#### *5.8.5.2 Rotary mode off-axis (Option Code -010)*

Unless otherwise specified, all values are valid before EoL calibration and for all applications under following nominal performance conditions: Temperature range [-40, 150] °C, $v_{el}$ ≤ 50 krpm, Magnetic flux density |B| ≥ 10 mT.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| XZ – Intrinsic Linearity Error, IMC | $LE_{\_IMC\_XZ}$ | -2.0 | | 2.0 | deg | |
| YZ – Intrinsic Linearity Error, IMC | $LE_{\_IMC\_YZ}$ | -2.0 | | 2.0 | deg | |
| XZ, YZ – Total Drift, IMC | $\partial\theta_{TT\_XZ\_YZ}$ | -0.8 | | 0.8 | deg | $T_{RT}$ = 35 °C |
| Magnetic Hysteresis, IMC Mid-field | $\theta_{EMH\_IMC\_MF}$ | | | 0.2 | deg | Rotary Mode (Midfield variant) |
| Angular noise, RMS | $\theta_{STD}$ | | 0.04 | | deg | *DSP_LFC_HI* = 0 |
| | | | 0.10 | | deg | *DSP_LFC_HI* = 3 |

*Table 22: Accuracy specifications for rotary mode off-axis at limited performance conditions*

#### *5.8.5.3 Stray field immune rotary mode (Option Code -600)*

Unless otherwise specified, all values are valid before EoL calibration and for all applications under the following conditions: Temperature range [-40, 150] °C, vel ≤ 50 krpm, Magnetic flux gradient ΔBz/ΔXY ≥ 10 mT/mm.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| XY - Intrinsic Linearity Error, dBz | $LE_{\_DBZ\_XY}$ | -1.4 | | 1.4 | deg | |
| XY - Total Drift, dBz | $\partial\theta_{TT\_DBZ\_XY}$ | -1.0 | | 1.0 | deg | $T_{RT}$ = 35 °C |
| Stray Field Immunity | $\theta_{SF}$ | -0.40 | | 0.40 | deg | QFN-24 (Package Code: LW) In accordance with ISO11452- 8:2015, at 30 °C with stray field of 4 kA/m from any direction |
| | | -0.70 | | 0.70 | deg | TSSOP-16_EP (Package Code: GO) In accordance with ISO11452- 8:2015, at 30 °C with stray field of 4 kA/m from any direction |
| Angular noise, RMS | $\theta_{STD}$ | | 0.05 | | deg | *DSP_LFC_HI* = 0 |
| | | | 0.15 | | deg | *DSP_LFC_HI* = 3 |

*Table 23: Accuracy specification for stray field immune mode at limited performance conditions*

# 6 Functional description & interfaces

## 6.1 System Description

The MLX90382 is a high-speed magnetic position sensor designed for absolute and incremental rotary position sensing. The block diagrams are shown in Figure 2 and Figure 3. The primary signal processing blocks of the position sensor consist of the Triaxis Hall elements, signal multiplexing and amplification, the Analog-To-Digital Conversion (ADC), the Digital Signal Processing (DSP) and output interfaces providing the output signals.

## 6.2 Function Description

### 6.2.1 Overview

The MLX90382 supports the following features:

- Automatic gain control.
- Factory trimmed magnetic compensations for offset and I/Q gain mismatch over temperature in all magnetic modes.
- Computation for 16-bit angular position and 16-bit speed values with adjustable noise suppression or step responses. This includes an adjustable filter bandwidth and overshoot in the angular domain, ranging between 500 Hz to 100 kHz. An optional adaptive loop filter (ALF) optimizes the filter bandwidth, balancing noise suppression and regulation offset (due to magnetic acceleration). The upper and lower bandwidth limits are adjustable by the customer.
- Angular linearization using 16 equidistant correction points over 360 degrees, with linear interpolation. The 16-Point linearization can be calibrated by the customer at low speeds or in static conditions and functions independently from the filter setting across the full-speed range.
- Processing delay compensation for both internal and external delays (adjustable by the customer) by compensation of the speed-dependent angular offset. The signal processing timing specifications are listed in Table 12.
- Flexible signal conditioning for the 16-bit angular output, allowing:
    - Selection of input range (clamping),
    - Adjustment of angular offset,
    - Definition of output range for transmission via SPI, SSI and PWM interfaces,
    - Specification of a fault band value to indicate a safe state.

### 6.2.2 Temperature Sensing

The MLX90382 provides onboard temperature sensing, which can be read out via *TEMP[11:0]*. The physical value is encoded as defined in the SENT standard, Section A.5.3.2, in the range [200 : 0.125 : 711.875] [K].

$$T[°C] = \frac{TEMP[11:0]}{8} + 200[K] - 273.15$$

### 6.2.3 Digital Signal Processing

After the 14-bit digitalization of the analog I/Q signals, they are conditioned by factory calibrated, temperature-dependent offset compensation, as well as sensitivity and orthogonality correction. The customer can access intermediate processing values via DSP registers (see Section 9.3). The signal processing chain is illustrated in Figure 7. Compared to the output angle at the interface, these values have an internal update frequency of $f_{ac}/26$. The sensitivity, orthogonality and offset compensated I/Q values can be read-out as averaged values trough *GC_I*[15:0] and *GC_Q[15:0].* The averaging window used to calculate the mean $\overline{GC\_X}$ is configured by *DSP_GC_AVG[4:2]* as follows:

$$\overline{GC\_X} = \begin{cases} \dfrac{GC\_X}{4^{\,DSP\_GC\_AVG[4:2]}}, & DSP\_GC\_AVG[4:2] < 7 \\ \dfrac{GC\_X}{8}, & DSP\_GC\_AVG[4:2] = 7 \end{cases}$$

To read out valid averages of the I-Channel, $\overline{GC\_I}_{corr}$ , by setting $DSP\_GC\_AVG[4:2] > 0$, the measured average $\overline{GC\_I}$ must be retrospectively corrected using the following calculation:

$$\overline{GC\_I}_{corr} = \begin{cases} \overline{GC\_I} \cdot \dfrac{4^{DSP\_GC\_AVG[4:2]} + 1}{4^{DSP\_GC\_AVG[4:2]}}, & 1 \le DSP\_GC\_AVG[4:2] < 7 \\ \overline{GC\_I} \cdot \dfrac{9}{8}, & DSP\_GC\_AVG[4:2] = 7 \end{cases}$$

When *DSP_GC_AVG[4:2]* > 0, the start of the averaging can be triggered by reading out GC_Q. The averaged values can then be accessed via GC_I and GC_Q after the waiting period of $t_{avg}$, calculated as:

$$t_{avg} = \begin{cases} DSP\_GC\_AVG[4:2] \cdot \dfrac{26}{f_{ac}}, & DSP\_GC\_AVG[4:2] < 7 \\ 8 \cdot \dfrac{26}{f_{ac}}, & DSP\_GC\_AVG[4:2] = 7 \end{cases}$$

The angular phase and speed are tracked using a phase tracking loop, which operates by monitoring an error signal derived from the I/Q signals. The integration time is configurable to balance noise suppression and dynamic performance (refer to Section 6.2.4). The linearized phase can be read from register *LIN_PHASE[15:0]*, and the 16-bit speed value can be read via *SPEED[15:0]*. The phase tracking is followed by the compensation of internal processing delays. The delay-compensated values, accessible through *DRIFTC_PHASE[15:0]*, include an optional angular offset that can be applied via *PHASE_OFS[15:0]* for zero-angle calibration. Signal conditioning allows the adaptation of the internal 16-bit angle value to the bit width required by the output protocol. Before the angular value is provided as DSP_DATA to the output interface, its update frequency is scaled up to $f_{ac}$ by linear interpolation.

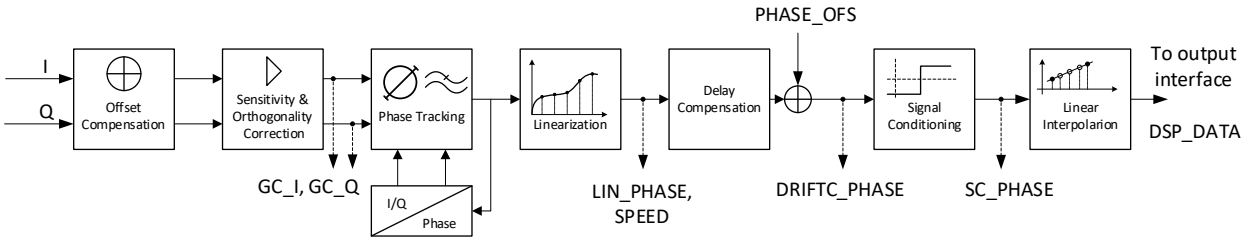



*Figure 7: Digital signal processing architecture*

### 6.2.4 High-Dynamic Performance

The phase tracking loop filter can be adapted via parameter to match application-specific dynamic behaviour. The two parameters are loop filter constant (LFC) and the step response overshoot (OS). The registers *DSP_LFC_LO[10:8]* and *DSP_LFC_HI[13:11]* define the range of LFC for automated bandwidth adaption. Setting both registers to the same value disables the automated adaptation. The overshoot is configured via *DSP_SROS[15:14]*.

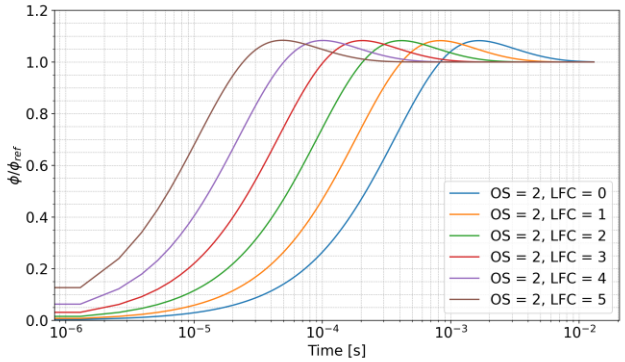



*Figure 8: Step response $\phi/\phi_{ref}$ over loop filter bandwidth LFC at $f_{AC}$ = 20 MHz*

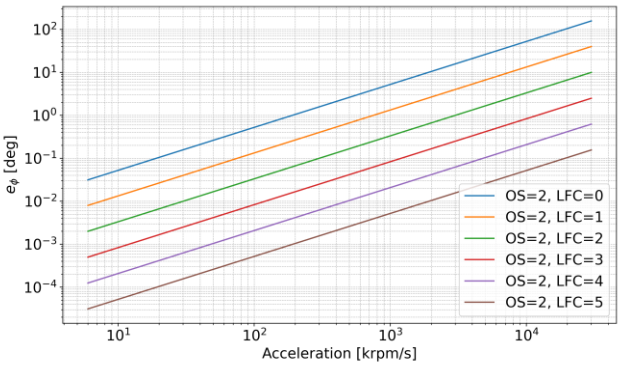



*Figure 9: Angular error $e_\phi$ over acceleration and loop filter bandwidth LFC at $f_{AC}$ = 20 MHz*

The step response behaviour and the angular error due to acceleration at different LFC and OS values are shown Figure 8 and Figure 9, using simulated results.

| OS | Overshoot (%) |
|---|---|
| 0 | 2.7 |
| 1 | 5.1 |
| 2 | 8.9 |
| 3 | 15.2 |

*Table 24: Overshoot in % over OS*

| LFC | Cutoff frequency $f_{-3dB}$ (Hz) * $f_{AC}/f_{RCO}$ | | | |
|---|---|---|---|---|
| | OS = 0 | OS = 1 | OS = 2 | OS = 3 |
| 0 | 495 | 509 | 539 | 595 |
| 1 | 990 | 1020 | 1079 | 1193 |
| 2 | 1989 | 2049 | 2168 | 2396 |
| 3 | 4010 | 4132 | 4374 | 4835 |
| 4 | 8158 | 8410 | 8906 | 9852 |
| 5 | 16914 | 17450 | 18500 | 20498 |

*Table 25: Cut-off frequency over LFC and OS*

### 6.2.5 I/Q Amplitude and Orthogonality Calibration

The sensitivity and orthogonality between the I-channel and Q-channel are factory calibrated but can change in an integrated module. A common example is off-axis positioning of the IC with different field amplitudes in X-Y and Z directions. The relative sensitivity and orthogonality between the I-channel and Q-channel can be adjusted via *S_QQ[15:0]* and *S_IQ[15:0]*, respectively, minimizing the angular error over a full electrical period before applying the 16-Point Linearization. This correction is applied to the GC_I and GC_Q values (see Figure 7) during the sensitivity and orthogonality correction step as follows:

$$\begin{bmatrix} GC_I \\ GC_Q \end{bmatrix} = \begin{bmatrix} 1 & S\_IQ/2^{15} \\ 0 & S\_QQ/2^{15} \end{bmatrix} * \begin{bmatrix} I \\ Q \end{bmatrix}$$

### 6.2.6 16-Point Linearization and Zero Position Adjustment

The 16-Point Linearization feature allows compensation for angular deviations caused by asymmetries in the sensor system, which includes the magnet and the sensor IC. The 8-bit signed equalization values (PEQ00[7:0]

to PEQ15[7:0]) define an angular error curve at angular sample points of 360/16 degrees * [00 .. 15]. All intermediate values are linearly interpolated, as shown in Figure 10. After equalization, the residual error curve is the difference between the input error curve and the interpolated equalization curve. The angular error curve should be measured with quasi-static rotation.

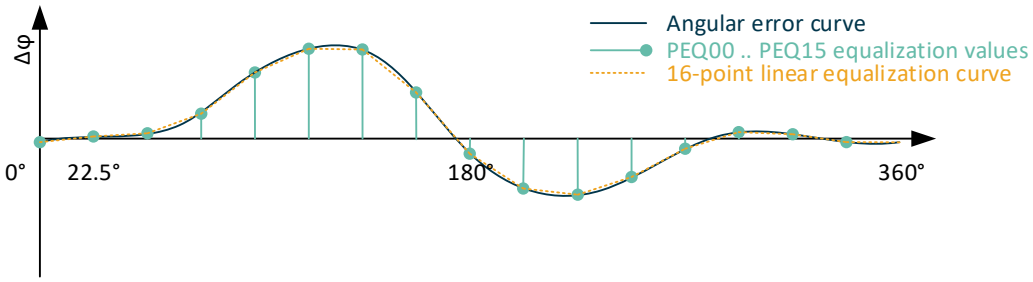



*Figure 10: 16-point linearization of angular error curve*

The equalization strength versus resolution can be adjusted using *PEQ_GAIN[2:0]*. If *PEQ_GAIN* is set to 0, no equalization is applied. For *PEQ_GAIN[2:0]* = [1..7], the error curve is adjusted per sample point as follows:

$$\Delta\varphi(xx) = singed(PEQxx[7:0]) * 2^{PEQ\_GAIN[2:0]-17} * 360[deg.]$$

The signed equalization values *PEQ00[7:0]* to *PEQ15[7:0]* range from -127 to 127. Table 23 details the equalization range and resolution for each sample point. In Figure 12, the adjustable range for the programmable linearization is illustrated.

| PEQ_GAIN[2:0] | Resolution [deg] | Range (+/-) [deg] |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0.0055 | 0.70 |
| 2 | 0.011 | 1.40 |
| 3 | 0.022 | 2.79 |
| 4 | 0.044 | 5.58 |
| 5 | 0.088 | 11.16 |
| 6 | 0.176 | 22.32 |
| 7 | 0.352 | 44.65 |

*Table 26: Equalization range and resolution per sample point for PEQ_GAIN*

Additionally, the angle of the magnet that results in a zero output value can be adjusted by setting the field *PHASE_OFS[15:0]*. This value is systematically added to the position value calculated by the phase tracking loop. This compensation should be applied after the linearization step.

### 6.2.7 Delay Compensation

The speed signal provided by the phase tracking loop is used to compensate for phase errors caused by system latency in case of angular speed. The compensation can be disabled by setting *DSP_DRIFTC_DIS[5] = 1.* Furthermore, the register *DELAY_CUS[7:0]* can be used to compensate for additional delays, such as related to filter networks in between the MLX90382 and the ECU, in steps of (26/64)/$f_{RCO}$.

### 6.2.8 Signal Conditioning

Signal conditioning allows the adaptation of output protocols such as SPI, SSI, and PWM by configuring the signalling range to match the desired output angle, using configurable parameters: *SC_Y1[15:0] and*

*SC_Y2[15:0]*. The input is the 16-bit measured angle value DRIFTC_PHASE (see Figure 7), after delay compensation and phase offset adjustment. It represents the electric angle over 360° range. Figure 11 illustrates the calculation steps of the signal conditioning procedure.

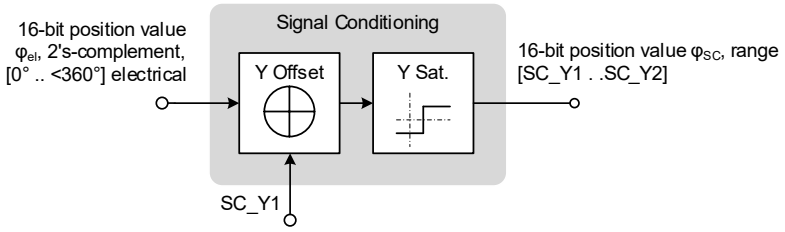



*Figure 11: Signal conditioning functional block diagram*

The output stage, defined by 2's-complement values SC_Y1 and SC_Y2, adds the offset SC_Y1 and saturates any values exceeding the output range [min(SC_Y1, SC_Y2), max(SC_Y1, SC_Y2)]. If SC_Y1 > SC_Y2, the transfer characteristic will be inverted. The signal conditioning process can be bypassed by setting [SC_Y1, SC_Y2] to [0,0] or [0, $2^{16}$-1]. The resolution of the angle after signal conditioning ($\Delta\varphi_{sc}$) can be calculated as:

$$\Delta\varphi_{sc}[deg.] = \frac{360}{2^{16}} * \max\left(1, \frac{2^{16}-1}{|SC_{Y2} - SC_{Y2}|}\right)$$

*SC_YE[15:0]* defines the fault band range. All safety related topics are described in the MLX90382 safety manual. Figure 12 shows an example with limitation at the input range and defined output range including a fault band.

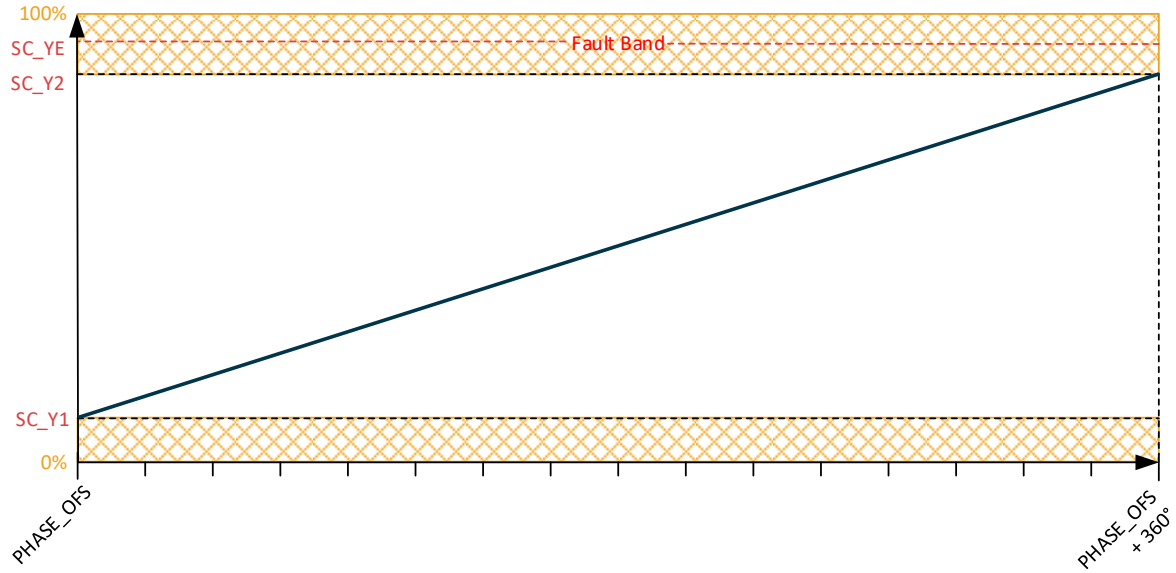



*Figure 12: Application with signal conditioning*

## 6.3 IO Interface Description

The interface stage features several input and output channels that can be selected by customers according to Table 3: QFN-24 package pinout and Table 4: TSSOP-16_EP package pinout.

### 6.3.1 Input channel specification

Each input channel contains an optional low-pass filter with cut-off frequency $INP_{LPF3dB}$ to further improve EMC robustness. The filter can be individually enabled on CS, MOSI, and SCLK by setting *PHY_RC_EN[2:0]*. The specifications for the input channels are listed in Table 27.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Input Low Voltage Detection Level | | 25.0 | 35.0 | 42.0 | % $V_{DD}$ | |
| Input High Voltage Detection Level | | 52.0 | 60.0 | 75.0 | % $V_{DD}$ | |
| Input Hysteresis Level | | 18.0 | 25.0 | 42.0 | % $V_{DD}$ | |
| Input Voltage Range | | 0 | | 100 | % $V_{DD}$ | |
| Input EMC Filter Cut-Off Frequency | $INP_{LPF3dB}$ | 3.5 | 6.0 | 10.5 | MHz | Setting *PHY_RC_EN[2:0]* to enable EMC filter. |

*Table 27: Input channel specifications*

### 6.3.2 Output channel specification

The output driver for the GPIO and the AU/BV/IW pins can be configured in different modes listed in Table 28 with *GPIO_CFG[10:9]* and *ABI_CFG[15:14]*. Each output pin voltage ranges from 0 V to VDD external supply.

| GPIO_CFG[10:9]/ABI_CFG[15:14] | Output Driver Mode |
|---|---|
| 00 | Hi-Z |
| 01 | Open drain p-MOS |
| 10 | Open drain n-MOS |
| 11 | Push-pull |

*Table 28 Output driver modes*

### 6.3.3 Interface selection for QFN-24

The interface function of the GPIO, AU_N, SCLK, MOSI and AU/BV/IW pins can be selected by setting *GPIO_IF[4:3] and ABI_IF[5]*. If CS is set to low, the SPI communication is activated without considering the interface selection in *GPIO_IF[4:3]*.

| Mode | GPIO_IF | ABI_IF | AU | BV | IW | GPIO | CS | AU_N | SCLK | MOSI |
|---|---|---|---|---|---|---|---|---|---|---|
| A0 | x | 1 | A | B | I | SPI: MISO | 0 | Hi-Z | SPI: SCLK | SPI: MOSI |
| A1 | x | 0 | U | V | W | SPI: MISO | 0 | Hi-Z | SPI: SCLK | SPI: MOSI |
| A0 | 2 | 1 | A | B | I | Hi-Z | 1 | Hi-Z | SPI: SCLK | SPI: MOSI |
| A1 | 2 | 0 | U | V | W | Hi-Z | 1 | Hi-Z | SPI: SCLK | SPI: MOSI |
| A2 | 1 | 1 | A | B | I | SSI: Data | 1 | Hi-Z | SSI: SCLK | - |
| A3 | 1 | 0 | U | V | W | SSI: Data | 1 | Hi-Z | SSI: SCLK | - |
| A4 | 0 | 1 | A | B | I | PWM | 1 | A_N | B_N | I_N |
| A5 | 0 | 0 | U | V | W | PWM | 1 | U_N | V_N | W_N |

*Table 29: Interface mode selection for QFN-24*

### 6.3.4 Interface Selection for TSSOP-16_EP

In the TSSOP-16_EP package, the interface pins are allocated differently compared to the QFN-24 package. Table 30 provides an overview of the pin function configuration. The interface configuration must be set individually for each of the two IC's inside the TSSOP-16_EP package.

| Mode | GPIO_IF | GPIO | CS | SCLK | MOSI |
|---|---|---|---|---|---|
| A0 | 2 | SPI: MISO | 1 | SPI: SCLK | SPI: MOSI |
| A0 | 2 | SPI Bus Mode (High-Z) | 0 | SPI: SCLK | SPI: MOSI |
| A1 | 1 | SSI: Data | 0 | SSI: SCLK | - |
| A2 | 0 | PWM | 0 | - | - |

*Table 30: Interface mode selection for TSSOP-16_EP*

## 6.4 SPI Slave Interface Description

### 6.4.1 General Description

The SPI slave interface for customer programming allows read/write access to all registers and memories, including the sensor position data. It operates up to 10 MHz SPI clock full-duplex and is designed to support functional safety, continuous readout, and multi-slave synchronization. The SPI supports all standard clock and phase modes for data exchange, which can be selected using *SPI_MODE[11:10]*.

### 6.4.2 SPI Timing Specifications

The capacitance $C_L$ refers to the max. load on the signal wire. (see Section 7).

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| SPI Clock Frequency | $f_{SCLK}$ | 0.04 | | 10.0 | MHz | *PHY_RC_EN[2:0]* = 0 (Input EMC Filter Off), 5 V mode, $C_L \leq 20$ pF |
| | | 0.04 | | 6.5 | MHz | *PHY_RC_EN[2:0]* = 0 (Input EMC Filter Off), 3.3 V mode, $C_L \leq 50$ pF |
| | | 0.04 | | 4.0 | MHz | Input EMC Filter On (Setting *PHY_RC_EN[2:0]*), $C_L \leq 50$ pF |
| SPI Idle time | $SPI_{tIDLE}$ | 1.0 | | | $1/f_{SCLK}$ | Idle time between consecutive SPI transactions. $\overline{CS}$ is at high state. |
| SPI CS inactive delay after SCLK active edge | $SPI_{tCS1}$ | 4.0 | | | $1/f_{AC}$ | SPI Write |
| | | 1.0 | | | $1/f_{AC}$ | SPI Read and SPI Frame Read |
| SPI CS active until SCLK active edge delay | $SPI_{tCS0}$ | 0.5 | | | $1/f_{SCLK}$ | *SPI_DBNC_CS[7:4]* = 0, *SPI_DBNC[11:8]* = 0 |
| SPI MISO disable delay after CS_B rising edge | $SPI_{tOD}$ | | | 100.0 | ns | |
| SPI MISO enable delay after CMD byte | $SPI_{tOE}$ | | | 100.0 | ns | *SPI_DBNC_CS[7:4]* = 0, CMD OK |
| MISO Data Delay | $SPI_{tSDO}$ | | | 40.0 | ns | $C_L$ = 20 pF, SCLK edge to MISO 70 % VDD for 5 V mode. |
| | | | | 80.0 | ns | $C_L$ = 50 pF, SCLK edge to MISO 70 % VDD for 3.3 V mode. |
| MOSI Setup Time | $SPI_{tSU\_MOSI}$ | 0.25 | | | $1/f_{SCLK}$ | *SPI_DBNC[11:8]* = 0 |
| MOSI Hold Time | $SPI_{tHD\_MOSI}$ | 0.25 | | | $1/f_{SCLK}$ | *SPI_DBNC[11:8]* = 0 |

*Table 31: SPI timing specification*

### 6.4.3 SPI Transaction for Register Read/Write Access

Data exchange is possible with three different SPI protocol variants: Register Read (RR), Register Write (RW) and Frame Read (FR). The structure of the protocols is shown in Figure 15. All transactions start with a command byte followed by an optional address byte. For Register Read and Register Write, the 6-bit command pattern shall match exactly. In case of mismatch, the device always responds as in Frame Read mode. RR and RW modes are active while CS = 0 ignoring the *GPIO_IF[4:3]* setting. Using FR mode needs a configuration of *GPIO_IF[4:3]* = 2 (SPI-Bus mode). The address byte ADR refers to the IC address space shown in Section 9. As the LSB of the 9-bit address ADR is always "0", only the upper 8-bit part of the address is used for RR, RW and FR operations.

#### *6.4.3.1 Register Read (RR)*

The register read operation begins by sending the command byte, followed by the aligned address byte. An optional third byte can be used to adjust the word alignment of the data transfer, which can be enabled using the *SPI_DMY[12]* bit. The subsequent byte is a dummy byte. The signal timing constraints for the register read operation are shown in Figure 13.

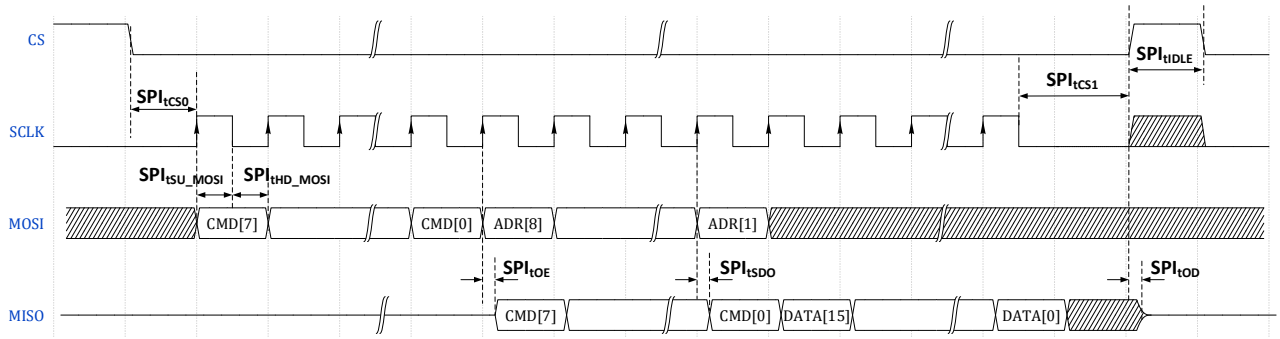



*Figure 13: Timing for SPI Register Read with SPI Mode 1 (CPOL = 0, CPHA = 1)*

Multiple bytes can be read sequentially during EOL calibration and non-safety related applications, this read option must not be used for safety related applications (e.g. ASIL, SIL). The multiple bytes read enables a fast and efficient communication. Starting from the provided address, multiple bytes can be read sequentially. The register *DE_SR[2:0]* = 3 must be set before reading a larger number of registers. Once the read attempt is complete, the register must be reset to its default value. The angular value must not be used during this procedure.

| Register | Address | Bit | R/W | Default | Description |
|---|---|---|---|---|---|
| **DE_SR** | 0x09C | [2:0] | R/W | 0 | Disable Shadow Register Monitor. If 3, register monitor is disabled. |

*Table 32: MLX90382ABA NVRAM address for shadow register monitor*

#### *6.4.3.2 Register Write (RW)*

The register write operation begins by sending the command byte, followed by the aligned address byte. This allows access to all device registers. Multiple registers can be written sequentially, starting from the provided address. The signal timing constraints for the register write operation are shown in Figure 14.

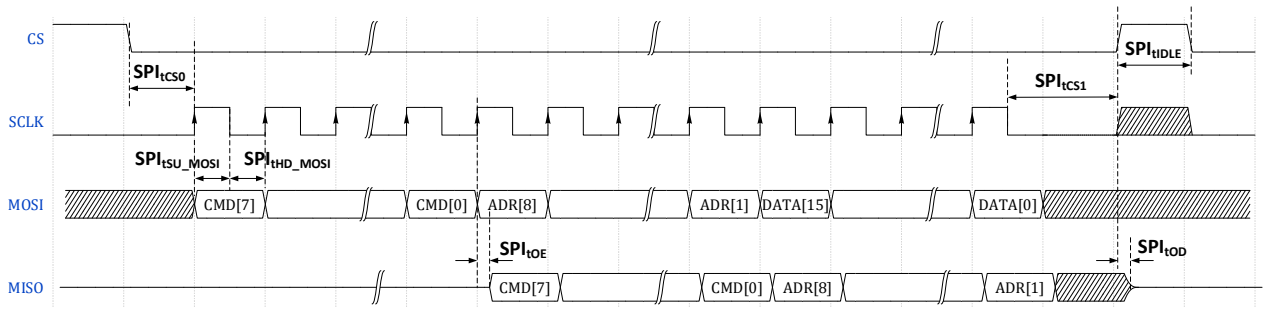



*Figure 14: Timing for SPI Register Write with SPI Mode 1 (CPOL = 0, CPHA = 1)*

#### *6.4.3.3 Frame Read (FR)*

When operating in Frame Read (FR) mode, the device transmits the content of up to four register addresses. This transmission can be initiated by an optional Frame Start (FS) byte and terminated by an optional CRC-8 byte. The FS byte is enabled via the *SPI_FRFSEN[4]* bit and consists of a configurable content (*SPI_FRSF[3:0]*) and a rolling counter. The rolling counter, which defines a nibble of the optional FS byte, allows the ECU to detect desynchronization that may result from lost SCLK edges. The composition of the FS byte is shown in Table 33.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Content | SPI_FRSF | | | | Rolling Counter | | | |

*Table 33: Frame start byte in Frame Read*

The second byte of the FR frame is ignored but still transmitted to prevent bus congestion in half-duplex mode and to allow command fail checks by the ECU. An optional third dummy byte can be enabled via *SPI_DMY[13]* to adjust the word alignment of the data transfer. The content of register addresses for readout can be configured by setting *SPI_FADDR0..3*. If *SPI_FADDR0[7:0]* is set to 0x00, the angular value will be transmitted (see Section 6.4.4.1). If one of the *SPI_FADDR1..3* register is set to 0x00, its content will not be transmitted and will not part of the frame. The length of the FR frame is defined as:

$$L_{Frame}[byte] = SPI\_FRFSEN + 2 \cdot (1 + (SPI\_FADDR1 > 0) + (SPI\_FADDR2 > 0) + (SPI\_FADDR3 > 0)) + SPI\_FRCRCEN.$$

The optional CRC-8 byte, which can be activated using *SPI_FRCRCEN[5]*, protects the data fields. An additional method for detecting transmission errors is provided via binary inversion. By setting the bit position “x” in field *SPI_FRINV[9:6],* the byte of content DATA(FADDR”x”) will be binary inverted. A comparison between inverted and non-inverted DATA allows error detection.

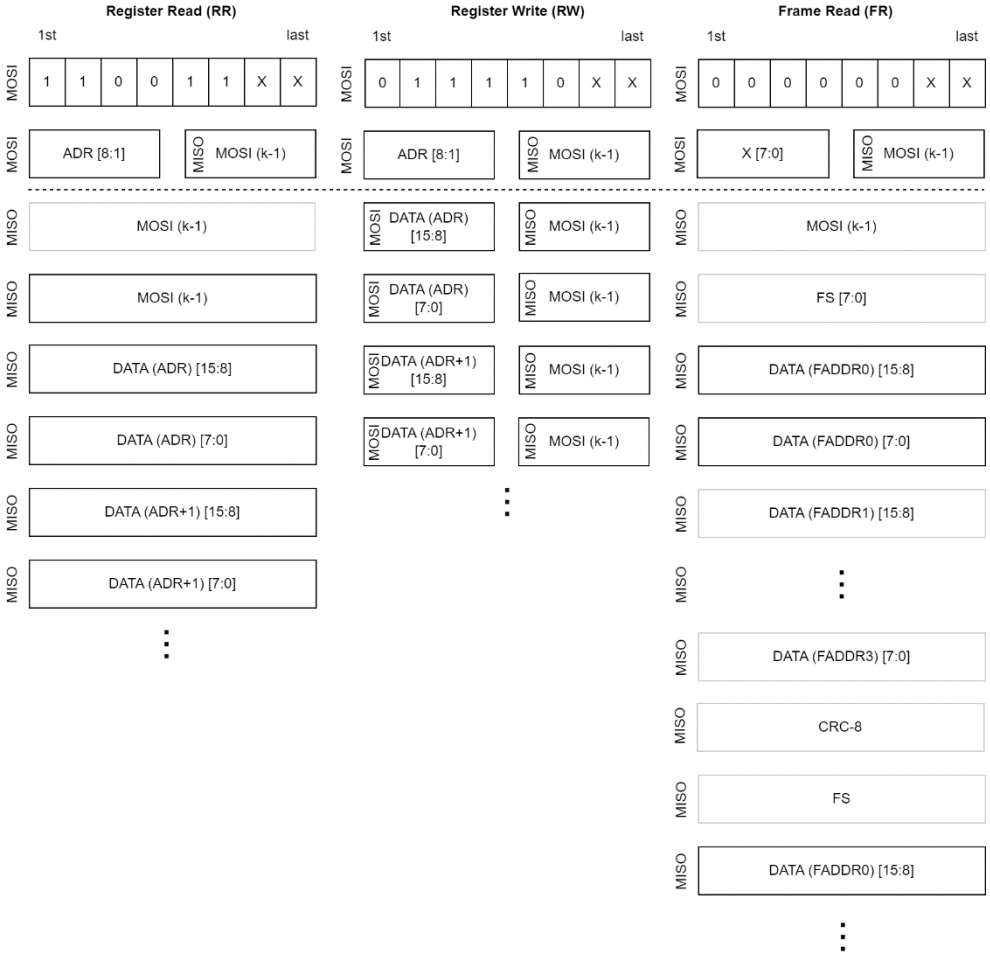



*Figure 15: SPI Protocols for Read/Write and Frame Read*

## 6.4.4 SPI Data Sample Timing

### *6.4.4.1 Angle Data Sampling in Frame Read Mode*

By setting *SPI_FADDR0* = 0x00, the angle value is sampled from digital signal processing with a maximum distance of (*SPI_CPTLT[2:0]* + 0.5) * 1/$f_{SCLK}$ [s] before the DATA(FADDR0) word. To ensure compliance with bus timing requirements, it is necessary to adjust *SPI_CPTLT* accordingly:

$$SPI\_CPTLT \geq 5 \cdot \frac{f_{SCLK}}{f_{ac}} - 0.5$$

### *6.4.4.2 Data Sampling*

All registers, in FR mode for *SPI_FADDR0* != 0x00, will be captured in the beginning of the previous byte transfer.

## 6.4.5 SPI Transaction for Synchronous Read Access of Multiple Slaves

The SPI interface allows synchronous capturing and sequential transmission of angular data with multiple SPI slaves on a shared SPI interface. The Super Frame Read (SFR) mode defines a delayed transmission of the FR response frame, facilitating a time-division-multiple-access (TDMA) scheme on the MISO line. This setup supports up to 16 SPI slaves, allowing them to capture or measure synchronized data and transmit it sequentially on the shared MISO bus. This specific mode can only be used in combination with the SPI debounce register setting *SPI_DBNC[3:0]* = 2 for all MLX90382ABA slave devices. The debounce function introduces a delay between SPI master clock SCLK and the SPI slave MISO response, as described in Section 6.4.6. A common use case for the SFR is the Dual-Die product configuration in the TSSOP-16_EP package, as shown in Section 4.1.2. The SFR can be configured using the following options.

#### 6.4.5.1 Time-division multiple access via Super Frame Read mode

The time-division multiple access (TDMA) mechanism is controlled through *SPI_SFRDLY[15:8]* in the slave device(s). This configuration defines the delay, in bytes, between the start of the first byte in the SFR frame and the beginning of the specific slave device's first byte within the SFR frame.

#### 6.4.5.2 Angular capture point

The capture point of the angular value can be synchronized across all slave devices by setting *SPI_SFR_SCPT[3] = 1*. This ensures that the capture point is aligned with the position of the very first *DATA(FADDR0)[15:8]* byte within the entire Super Frame. To ensure synchronization, *SPI_CPTLT[2:0]* should be identical on all slave devices to capture the angular data at the same position before the first DATA(FADDR0)[ 15:8] in the Super Frame. If *SPI_SFR_SCPT[3]* = 0, the angular position is captured before each individual slave device's DATA(FADDR0)[15:8]. The synchronization options are illustrated in Figure 16 and the timing behaviour is described in Section 6.4.4.1.

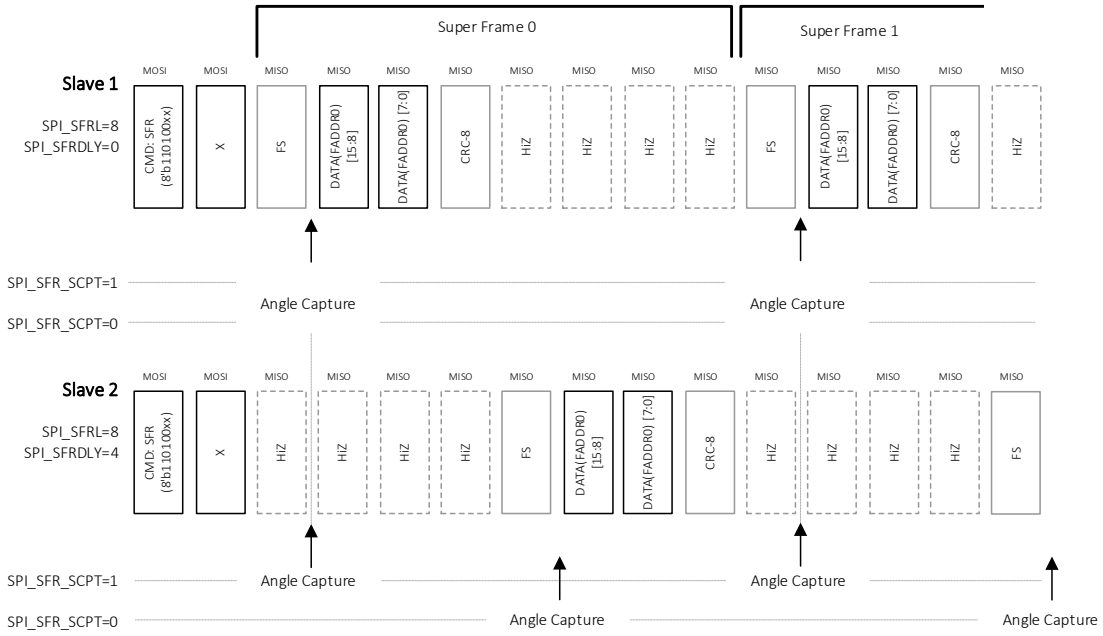



*Figure 16: Angle capture synchronization in Super Frame Mode*

#### 6.4.5.3 Super Frame length alignment

The Super Frame length ($L_{SFrame}$) must be set as the sum of all bytes composed of the individual frames (see Section 6.4.3.3) of each slave device, using *SPI_SFRL[7:0]*. The frame length of each slave can differ. The total frame length can be calculated as:

$$L_{SFrame}[byte] = SPI\_SFRL = \sum_{i=1}^{N} L_{Frame}(i)$$

### 6.4.6 SPI EMC debounce filter

The SPI inputs SCLK, CS and MOSI have dedicated digital symmetric debounce filter with programmable filter depth. *SPI_DBNC[11:8]* and *SPI_DBNC_CS[7:4]* configure the debouncing delay for SCLK ($\tau_{SCLK}$), MOSI ($\tau_{MOSI}$) and CS ($\tau_{CS}$) respectively as follows:

$$\tau_{CS}[s] = SPI\_DBNC\_CS[7:4] * \frac{2}{f_{RCO}}$$

$$\tau_{MOSI}, \tau_{SCLK}[s] = \frac{SPI\_DBNC[11:8]}{f_{RCO}}$$

It is important to consider that $SPI_{tOD}$, $SPI_{tOE}$ and $SPI_{tSDO}$ will accumulate with the defined debouncing delay. Next to this, the setting of *SPI_DBNC[11:8]* > 0 limits the maximum SCLK frequency.

## 6.5 SSI Output Description

In SSI mode, the angular value is transmitted as a 15-bit data word with in a 16-bit frame, with a clock period of T = $1/f_{SCLK}$. The angular value must be scaled to 15-bit using the signal conditioning function (see Section 6.2.8) by the following configuration, such that the MSB of the complete 16-bit SSI-frame always remains zero. The register value *SC_Y2[15:0]* must be set to *SC_Y2[15:0]* = 16'h7FFF, resulting in maximum transmitted angle value resolution of 15 bits.

A new angular value is only sampled after start-up or when the clock period T exceeds a minimum threshold, $T_M$. $T_M$ is the minimum time required by the slave to recognize that the data transmission is complete. It can be configured via *SSI_TM[12:5]* as follows:

$$T_M[s] = (SSI\_TM[12:5] + 1) \cdot \frac{8}{f_{ac}}$$

The pause time ($T_P$) must consider $T_M$ and a minimum idle time, such that: $T_P \geq T_M + 0.5$ µs. A Data line high level during the pause period $T_P$, following the timeout period $T_M$, requires a pullup resistor on the Data line, as shown in the recommended example application diagrams in Chapter 7.

If the ECU triggers 16 or more clocks (without any clock violation), the last transmitted word is repeated, starting with the MSB. The diagram in Figure 17 illustrates two consecutive readouts of the same angular value, followed by a third readout of a new angular value activated after a clock timing violation. The timing specifications are list in Table 31.

### 6.5.1 SSI Timing Specification

The capacitance $C_L$ refers to the max. load on the signal wire. (see Section 7)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| SSI Clock Frequency | $f_{SCLK}$ | 0.04 | | 10.0 | MHz | *PHY_RC_EN[2:0]* = 0 (Input EMC Filter Off), 5 V mode, $C_L \leq 20$ pF |
| | | 0.04 | | 6.5 | MHz | *PHY_RC_EN[2:0]* = 0 (Input EMC Filter Off), 3.3 V mode, $C_L \leq 50$ pF |
| | | 0.04 | | 4.0 | MHz | Input EMC Filter On (Setting *PHY_RC_EN[2:0]*), $C_L \leq 50$ pF |
| SSI Data Delay | $SSI_{tSDO}$ | | | 40.0 | ns | $C_L$ = 20 pF, SCLK rising edge to Data 70 % VDD for 5 V mode. |
| | | | | 80.0 | ns | $C_L$ = 50 pF, SCLK rising edge to Data 70 % VDD for 3.3 V mode. |

*Table 34: SSI timing specification*

### 6.5.2 SSI Data Sample Timing

The DSP output is sampled based on the configuration of *SSI_CPT[14]*, as listed in Table 35. If *SSI_CPT[14]* = 1, the data is always captured at the rising edge of $T_M$. Consequently, the age of the angular information in the next SSI clock sequence is $T_P$ - $T_M$. It should be noticed that the data at the first clock sequence after start-up contains no valid information, as no capture event was triggered before this point. In case *SSI_CPT[14]* = 0, the data is always captured at the first falling edge of SCLK.

| SSI_CPT[14] | Description | Condition |
|---|---|---|
| 0 | The data will always be captured at the first falling edge of SCLK | SCLK ≤ 2MHz |
| 1 | The data will always be captured after $T_M$ | |

*Table 35: Configuration of SSI angle capture point*

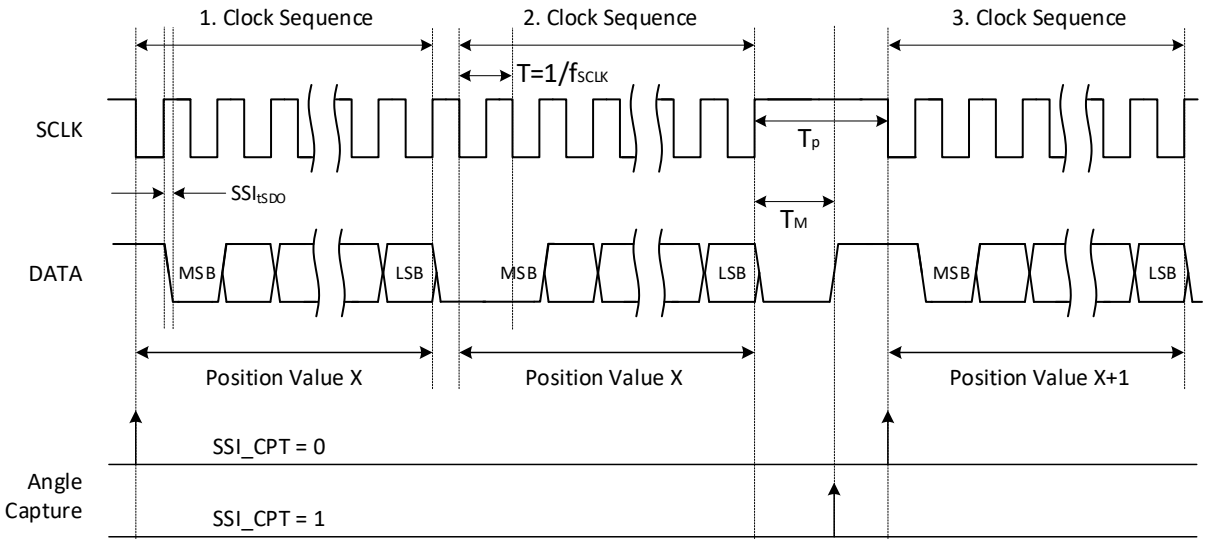



*Figure 17: SSI timing diagram*

### 6.5.3 SSI Interface Configuration

If SSI mode is selected by setting *GPIO_IF[4:3]* = 1, the register *SPI_MODE[11:10]* must be set to 1. If further SPI communication is required, the SPI master must be configured accordingly.

### 6.5.4 SSI Parity Bit

If *SSI_PARPOS[3:0]* < 9, an optional parity bit can be transmitted within the 16-bit frame. *SSI_PARPOS[3:0]* specifies the position of the parity bit within the 16-bit frame. The variable bit-position of the parity bit allows adjustment of the SSI frame width. The frame transmission can be stopped immediately after the transmission of the parity bit. It allows to adapt frame length. The SSI frame is composed as shown in Table 36, with the scaled angular value $\varphi_{sc}$ and the parity bit.

| Bit Position | 15 | 14 SSI_PARPOS+1 | SSI_PARPOS | SSI_PARPOS-1 0 |
|---|---|---|---|---|
| Content | 0 | $\varphi_{sc}[14: SSI\_PARPOS + 1]$ | Parity-Bit | to be ignored |

*Table 36: MLX90382ABA SSI frame composition with parity bit*

It can be seen that the information inside $\varphi_{sc}$ undergoes a bit shift: $\varphi_{sc} >> (SSI\_PARPOS + 1)$, which can be expressed as the operation: $floor\left(\frac{\varphi_{sc}}{2^{SSI\_PARPOS+1}}\right)$. This affects all related information, such as the angular value and in case of signal conditioning (refer to Section 6.2.8) the defined thresholds for SC_YE and SC_HL and the scaled output angle.

## 6.6 PWM Output Description

### 6.6.1 PWM Definition

The MLX90382 generates pulse width modulation (PWM) signals with a time resolution of $1/f_{AC}$. The interface supports a freely programmable period $T_{PWM}$, configured via *PWM_PERIOD[15:0]*:

$$T_{PWM} = \frac{PWM\_PERIOD[15:0]}{f_{AC}}$$

The PWM polarity can be inverted using the *PWM_INV[14]* bit.

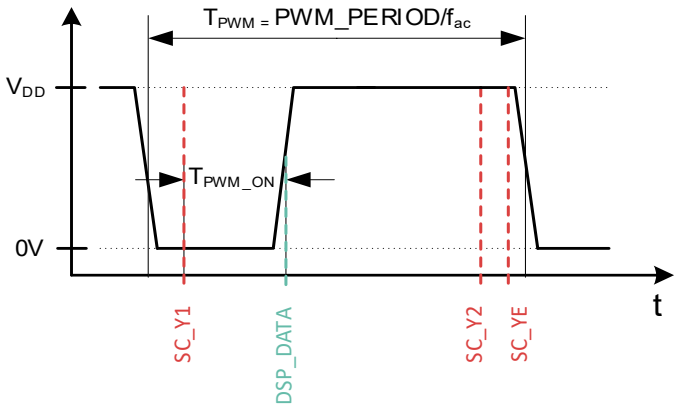



*Figure 18: PWM signal definitions with PWM_INV = 0*

The PWM duty cycle ($T_{PWM\_ON}$) is proportional to the angular value after signal conditioning and interpolation, which is captured at the beginning of each PWM period. The upper and lower limit of the on-time, $T_{PWM\_ON}$, are defined by the output of the signal conditioning via *SC_Y1[15:0]* and *SC_Y2[15:0]* (see Section 6.2.8). Figure 18 illustrates a PWM configuration, including the defined on-time. DSP_DATA represents the output data after interpolation (see Section 6.2.3). *SC_YE[15:0]* refers to the fault band indication that is described in the MLX90382 safety manual. It is important to note that the following constraint must be considered for setting the PWM period by *PWM_PERIOD[15:0]*:

$$PWM\_PERIOD[15:0] > max(SC\_Y1, SC\_Y2, SC\_YE)$$

The PWM Output resolution $R_{PWM}$ depends on the ratio between the application clock frequency and the PWM frequency and can be calculated as follows:

$$R_{PWM} = log2\left(\frac{f_{ac}}{f_{PWM}}\right)$$

To compensate for mismatch between rising and falling edge delays, the signed value *PWM_DC_OFS[8:0]* allows to adjust the $T_{PWM\_ON}$ time as follows:

$$\Delta T_{PWM\_ON} = \frac{PWM\_DC\_OFS[8:0]}{f_{ac}}$$

### 6.6.2 PWM performance characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| PWM Output Resolution | $R_{PWM}$ | | 12.0 | 16.0 | Bit | |
| PWM Frequency | $f_{PWM}$ | 305 | | 5000 | Hz | |
| PWM Frequency Tolerance | $\Delta f_{PWM}$ | -5.0 | | 5.0 | % $f_{PWM}$ | |
| PWM Duty Cycle Jitter | $J_{DC}$ | | | 0.03 | % | $f_{PWM}$ = 2 kHz; DC = 50 %, normalized to the period |
| PWM Period Jitter | $J_{PWM}$ | | | 500.0 | ns | $f_{PWM}$ = 2 kHz |

*Table 37: PWM performance characteristics*

## 6.7 ABI Incremental Encoder Output Interface

The MLX90382 features an incremental encoder output interface with three signals (see Figure 20). Signals A and B are quadrature signals, where the period represents an angular increment of $4 \cdot \Delta\theta$. The I signal is a reference signal that indicates one complete electrical revolution. In the positive rotation direction, the rising

edge of the I-channel marks the zero position, while in the negative direction, the falling edge indicates the zero position.

The direction of rotation is determined by the phase relationship between signals A and B, which corresponds to the sign of the angular velocity. When signal A leads signal B, the angular velocity is considered positive. If signal B leads signal A, the angular velocity is negative.

The ABI interface includes an adjustable hysteresis, which allows to balance noise versus accuracy (See Figure 19). The hysteresis can be configured over a wide range by *ABIUVW_HYS[13:10]*. The direction of rotation can be reversed using the *ABIUVW_DIR[9]* setting. It is recommended to set the hysteresis value higher than the expected peak noise. The hysteresis $HYS_{ABI\_UVW}$, expressed in degrees, can be calculated as follows:

$$HYS_{ABI\_UVW}[degrees] = \pm floor\left(2^{ABIUVW\_HYS[13:10]-1}\right) \cdot \frac{360}{2^{16}}$$

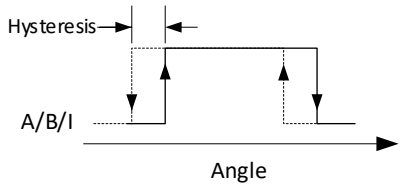



*Figure 19: ABI Hysteresis*

### 6.7.1 ABI performance characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Angular Resolution | $\Delta\theta$ | 0.18 | | | deg | *DSP_LFC_HI[13:11]*=0 Nominal Performance Condition |
| | | 0.35 | | | deg | *DSP_LFC_HI[13:11]*=0 Extended Performance Condition |

*Table 38: ABI performance characteristics*

### 6.7.2 ABI Configuration of Angular Resolution

The number of counts ($N_{ABI\_COUNTS}$) within one electrical revolution is defined by *ABI_LOG2N[3:0]* and the following equation:

$$N_{ABI\_COUNTS} = 4 \cdot 2^{ABI\_LOG2N[3:0]}$$

The maximum setting for *ABI_LOG2N[3:0]* is 12. The angular output resolution $\Delta\theta$ is defined by:

$$\Delta\theta[degrees] = \frac{360}{N_{ABI\_COUNTS}}$$

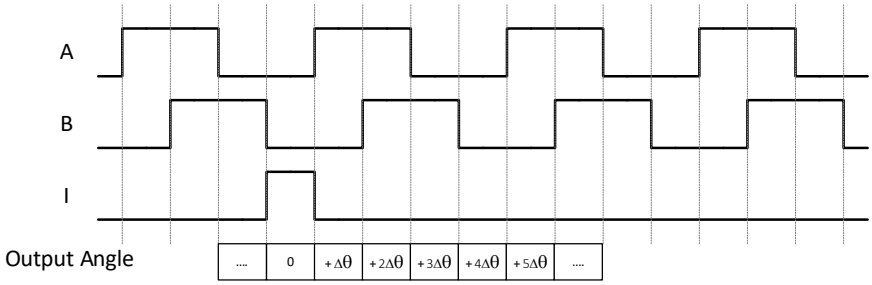



*Figure 20: ABI signal definition*

### 6.7.3 ABI Constraints on Configuration

The configuration of *ABI_LOG2N* and *ABIUVW_HYS* is constraint by the maximum angular speed ($v_{el}$). To ensure valid encoding of the ABI signals relative to angular speed, the following constraint must be considered:

$$\frac{max(v_{el}[rpm])}{f_{ac} * 60} 2^{16} < 2^{14-ABI\_LOG2N-ABIUVW\_HYS} - 1$$

The configuration of *ABI_LOG2N[3:0]* and *ABIUVW_HYS[13:10* is constrained also by the angular noise, which is influenced by the bandwidth of the internal tracking filter (refer to Section 6.2.4). The bandwidth is determined by the LFC settings, which must be considered when selecting the number of counts ($N_{ABI\_COUNTS}$). *ABI_LOG2N[3:0]* must be limited according to the setting in *DSP_LFC_HI[13:11]* and the operating performance conditions (refer to Section 5.8.1). The appropriate settings for *ABI_LOG2N[3:0]* in relation to *DSP_LFC_HI[13:11]* are provided in Table 39.

| | ABI_LOG2N[3:0] | |
|---|---|---|
| DSP_LFC_HI[13:11] | Nominal Performance Condition | Extended Performance Condition |
| 0 | 9 | 8 |
| 1 | 8 | 7 |
| 2 | 8 | 7 |
| 3 | 7 | 6 |
| 4 | 7 | 6 |
| 5 | 7 | 5 |

*Table 39: MLX90382ABA configuration of ABI_LOG2N in relation to DSP_LFC_HI*

## 6.8 UVW Output Interface

The MLX90382 UVW interface emulates the U, V and W signals typically generated by three Hall switches in Brushless DC (BLDC) motors. These three signals are electrically phase-shifted by 120 degrees and switch at the position where the mechanical angle indicates a pole change in the motor. The number of pole pairs $N_{pp}$ can be set from 1 to 32 pairs through $N_{pp}$ = *UVW_PP[8:4]* + 1.

Additionally, the MLX90382 includes a dedicated hysteresis setting, configurable via *ABIUVW_HYS[13:10].* It prevents incorrect transitions. This setting is adjustable over a wide range to optimize the balance between noise and accuracy. The calculation of the hysteresis $HYS_{ABI\_UVW}$ is detailed in Section 6.7.

The direction of rotation can be reversed by setting *ABIUVW_DIR[9].* Figure 21 shows and example of UVW signals with $N_{pp}$ = 3, along with the corresponding mechanical angle θ.

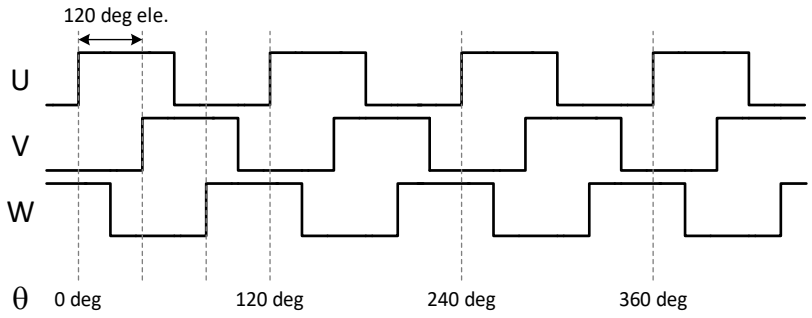



*Figure 21: UVW signal definition with 3 pole pairs*

### 6.8.1 UVW performance characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Number of pole pairs | $N_{pp}$ | 1 | | 32 | | |

*Table 40: UVW performance characteristics*

## 6.9 Differential ABI and UVW Output

The QFN-24 package provides a differential ABI and UVW interface output, meaning the ABI/UVW signals are logical inverted, with signal levels ranging between VSS and VDD. By configuring *GPIO_IF[4:3]* to 0, the inverted signals A/U_N, B/V_N and I/W_N are provided at the AU_N, SCLK and MOSI pins, respectively (see Table 29).

## 6.10 Functional Safety

According to IEC61508, the MLX90382ABA achieves SIL-2. The technical safety concepts are described in the safety manuals. In case of random internal failure detection, the MLX90382ABA transitions to one of its safe states: it either set its output in a high impedance state (Hi-Z), indicates safe state trough signal conditioning, or it write the status byte in SPI frames, as long as the failure is detected.

## 6.11 Temperature Offset Compensation

The correct application of the temperature offset correction values is essential for compliance with the angular accuracy specification, see Section 5.8. Incorrect values can result in increased angular error over the temperature range. Based on the selected sensing mode, see register *SENSING_MODE[2:0]*, the offset calibration values must be written to the NVRAM registers *OFS_TC_HOT_I/OFS_TC_COLD_I* and *OFS_TC_HOT_Q/OFS_TC_COLD_Q*. Table 41 specifies which content from specific NVRAM registers needs to be copied and permanently stored into the mentioned NVRAM registers according to the sensing mode. This procedure must be repeated whenever the sensing mode is changed. Table 42 lists the relevant NVRAM registers for this procedure. In the case of *SENSING_MODE[2:0]* = 0 (ROTARY_XY), initial reprogramming is not required, as the correct offset calibration values are already stored in the delivery state.

| Register | Content according to applied Sensing Mode | | |
|---|---|---|---|
| | ROTARY_XY (SENSING_MODE = 0) | ROTARY_XZy (SENSING_MODE = 1) | ROTARY_YZx (SENSING_MODE = 2) |
| **OFS_TC_COLD_I** | OFS_X_TC_COLD[7:0] | OFS_X_TC_COLD[7:0] | OFS_Y_TC_COLD[7:0] |
| **OFS_TC_HOT_I** | OFS_X_TC_HOT[15:8] | OFS_X_TC_HOT[15:8] | OFS_Y_TC_HOT[15:8] |
| **OFS_TC_COLD_Q** | OFS_Y_TC_COLD[7:0] | OFS_ZY_TC_COLD[7:0] | OFS_ZX_TC_COLD[7:0] |
| **OFS_TC_HOT_Q** | OFS_Y_TC_HOT[15:8] | OFS_ZY_TC_HOT[15:8] | OFS_ZX_TC_HOT[15:8] |

*Table 41: MLX90382ABA mapping of offset correction register according to sensing mode*

| Register | Address | Bit | R/W | Default |
|---|---|---|---|---|
| **OFS_TC_HOT_I** | 0x122 | [15:8] | R/W | OFS_X_TC_HOT[15:8] |
| **OFS_TC_COLD_I** | | [7:0] | R/W | OFS_X_TC_COLD[7:0] |
| **OFS_TC_HOT_Q** | 0x124 | [15:8] | R/W | OFS_Y_TC_HOT[15:8] |
| **OFS_TC_COLD_Q** | | [7:0] | R/W | OFS_Y_TC_COLD[7:0] |
| **OFS_X_TC_HOT** | 0x176 | [15:8] | R | |
| **OFS_X_TC_COLD** | | [7:0] | R | |
| **OFS_Y_TC_HOT** | 0x178 | [15:8] | R | |
| **OFS_Y_TC_COLD** | | [7:0] | R | |
| **OFS_ZX_TC_HOT** | 0x17A | [15:8] | R | |
| **OFS_ZX_TC_COLD** | | [7:0] | R | |
| **OFS_ZY_TC_HOT** | 0x17C | [15:8] | R | |
| **OFS_ZY_TC_COLD** | | [7:0] | R | |

*Table 42: MLX90382ABA: NVRAM map entries related to offset correction*

## 6.12 Sensitivity and Orthogonality Calibration Values

The correct application of the sensitivity and orthogonality calibration values is essential for compliance with the angular accuracy specification (see Section 5.8). The sensitivity and orthogonality calibration feature is discussed in Section 6.2.5. Incorrect values can result in increased angular error in different sensing modes. The following procedure is proposed to transfer selected, sensing mode-dependent sensitivity calibration data, stored in the NVRAM, into alternative NVRAM registers *S_IQ[15:0]* and *S_QQ[15:0]*. Reprogramming the calibration values for a specific sensing mode only needs to be done once (EoL). If the sensing mode is changed, the values must be adjusted again. In the case of *SENSING_MODE[2:0]* = 0 (ROTARY_XY), initial reprogramming is not required, as the sensitivity and orthogonality calibration values are already stored in the alternative NVRAM registers at delivery. The sensitivity and orthogonality calibration values must be read out according to the selected sensing mode and stored into the alternative NVRAM registers *S_IQ[15:0]* and *S_QQ[15:0]*. The mapping is shown in Table 43. If *SENSING_MODE[2:0]* is modified, the procedure has to be repeated. Table 44 lists the relevant NVRAM register for this procedure.

| Register | Content according to applied Sensing Mode | | |
|---|---|---|---|
| | ROTARY_XY (SENSING_MODE = 0) | ROTARY_XZy (SENSING_MODE = 1) | ROTARY_YZx (SENSING_MODE = 2) |
| **S_IQ** | S_XY | S_XZY | S_YZX |
| **S_QQ** | S_YY | S_ZZY | S_ZZX |

*Table 43: MLX90382ABA mapping of sensitivity and orthogonality correction register*

| Register | Address | Bit | R/W | Default |
|---|---|---|---|---|
| **S_IQ** | 0x11C | [15:0] | R/W | S_XY |
| **S_QQ** | 0x11E | [15:0] | R/W | S_YY |
| **S_XY** | 0x186 | [15:0] | R | |
| **S_XZY** | 0x18A | [15:0] | R | |
| **S_YZX** | 0x18C | [15:0] | R | |
| **S_YY** | 0x190 | [15:0] | R | |
| **S_ZZX** | 0x192 | [15:0] | R | |
| **S_ZZY** | 0x194 | [15:0] | R | |

*Table 44: MLX90382ABA: NVRAM map entries related to sensitivity and orthogonality correction*

# 7 Application information

## 7.1 Example application diagrams

### 7.1.1 MLX90382 in QFN-24 Package and 3.3 V supply

Figure 22 shows the application diagram for a QFN-24 package in 3.3 V supply mode. If necessary, Pull-up ($R_{PU}$) or Pull-down ($R_{PD}$) resistors can be added on the interface wiring. The capacitance $C_L$ refers to the parasitic capacitive load on the output signal.

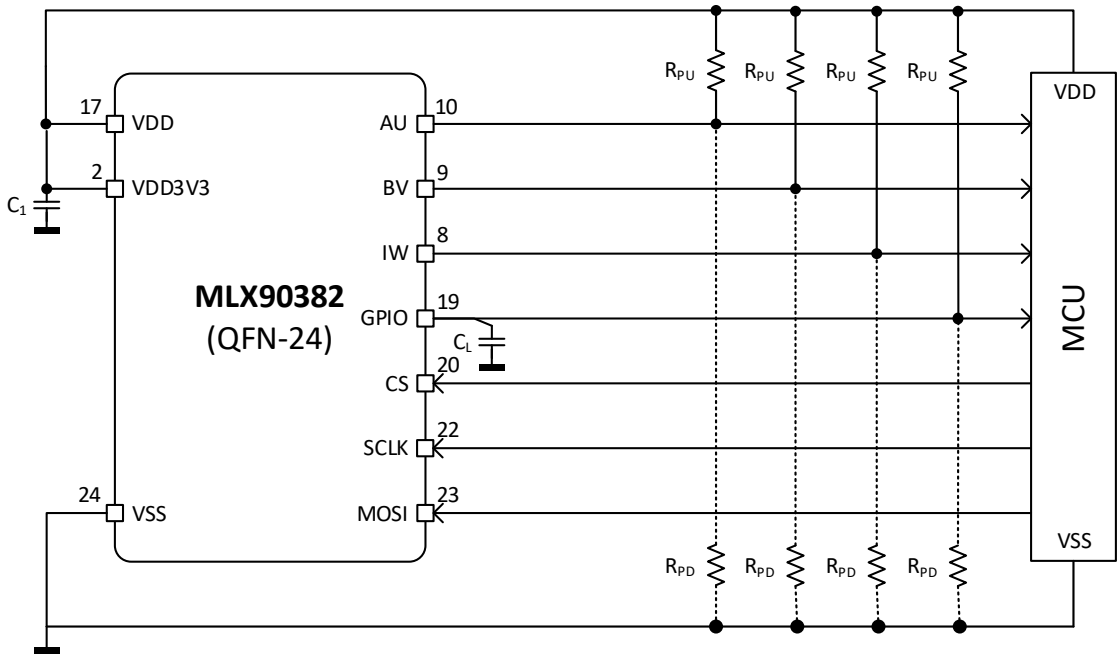



*Figure 22: Application example for QFN-24 with 3.3 V supply configuration*

| Component | Min. | Typ. | Max. | Unit | Comment |
|---|---|---|---|---|---|
| $C_1$ | | 330 | | nF | Close to the IC pin |
| $R_{PU}$/ $R_{PD}$ | 5 | | | kΩ | Push-pull mode. Applicable for all outputs. |
| $R_{PU}$/ $R_{PD}$ | 1 | | | kΩ | Open drain mode in 5 V mode<br>derived at 90 % VDD and 10 % VDD |
| | 2 | | | kΩ | Open drain mode in 3.3 V mode<br>derived at 90 % VDD and 10 % VDD |

*Table 45: Recommended component values for QFN-24 with 3.3 V configuration*

### 7.1.2 MLX90382 in TSSOP-16_EP Package and 5V supply

Figure 23 shows the application diagram for a TSSOP-16_EP package in 5 V supply mode. If necessary, Pull-up ($R_{PU}$) or Pull-down ($R_{PD}$) resistors can be added on the interface wiring. The capacitance $C_L$ refers to the parasitic capacitive load on the signal wire.

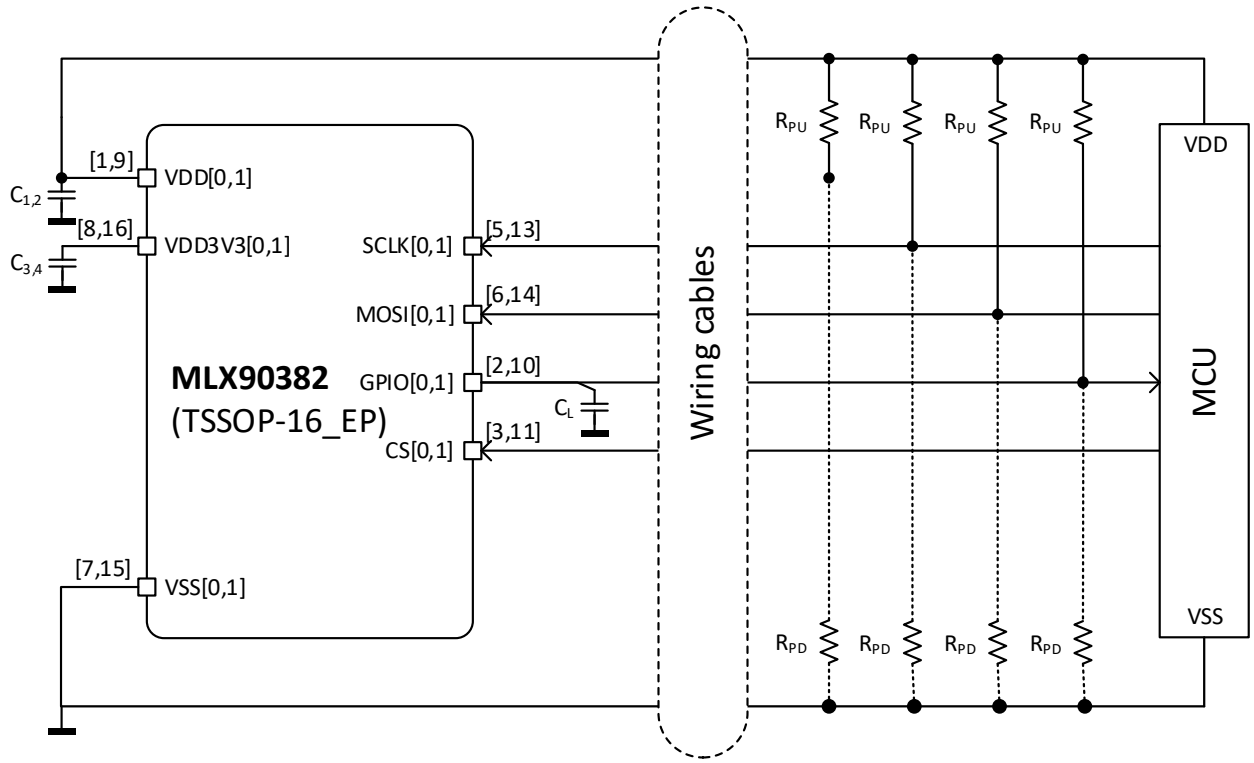



*Figure 23: Application example for TSSOP-16_EP with 5 V supply configuration*

| Component | Min. | Typ. | Max. | Unit | Comment |
|---|---|---|---|---|---|
| $C_1$, $C_2$ | | 330 | | nF | Close to the IC pin |
| $C_3$, $C_4$ | | 100 | | nF | Close to the IC pin, $C_3$, $C_4 \leq C_1$, $C_2$ |
| $R_{PU}$/ $R_{PD}$ | 5 | | | kΩ | Push-pull mode. Applicable for all outputs |
| $R_{PU}$/ $R_{PD}$ | 1 | | | kΩ | PWM open drain mode in 5 V mode derived to achieve 90 % VDD and 10 % VDD |
| | 2 | | | kΩ | PWM open drain mode in 3.3 V mode derived to achieve 90 % VDD and 10 % VDD |

*Table 46: Recommended component values for TSSOP-16_EP with 5 V configuration*

## 7.2 Application modes

### 7.2.1 Application Modes for Rotary Mode (Option Code -000 and -100)

From an application perspective, the different rotary modes correspond to the measurement of the angular position of the magnet as projected within one of the three planes defined by:

1. the X-Y, X-Zy or Y-Zx axis (option code -000),
2. or X-Y (option code -100)

of the spatial reference frame, as illustrated in the figures below. These modes can be configured with the setting in *SENSING_MODE[2:0].*

X-Y Mode | X-Zy Mode | Y-Zx Mode

*Figure 24: Exemplary illustration of the different rotary application modes*

### 7.2.2 Application Mode for Rotary Mode (Option Code -010)

A "through-shaft" off-axis configuration, as illustrated in Figure 25, can use the rotary mode in the X-Zy or Y-Zx plane to measure the shaft rotation.

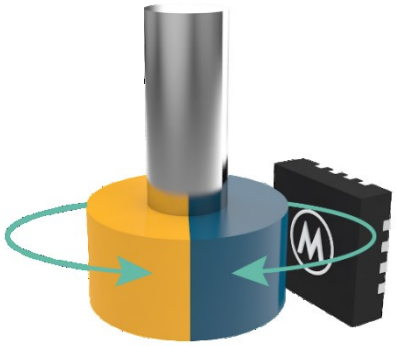


*Figure 25: Exemplary illustration of an applicative configuration exploiting the rotary mode (off-axis)*

### 7.2.3 Application Modes for Stray Field Immune Rotary Mode (Option Code -600)

For stray field immune configuration, the applicable rotary mode is the X-Y mode, illustrated in Figure 24.

### 7.2.4 Constraint on I/Q Amplitude Mismatch

Application scenarios such as off-axis application typically feature different amplitudes of the magnetic flux density in X/Y and Z direction. In off-axis application, the GC_I-Channel contains the magnitude in X-direction and the GC_Q-Channel the magnitude in Z direction. These output signals are described in Section 6.2.3. The

amplitude mismatch between I and Q can be compensated using the *S_QQ[15:0]* register, as detailed in Section 6.2.5. By setting S_QQ = $2^{15}$, the uncompensated amplitudes of GC_I and GC_Q can be measured as illustrated in Figure 26 by reading the registers *GC_I[15:0]* and *GC_Q[15:0]*.

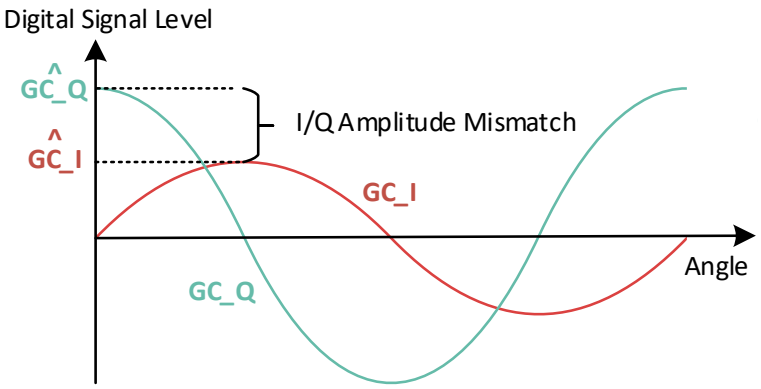



*Figure 26: Amplitude mismatch between I and Q*

By utilizing the uncompensated GC_I and GC_Q values, the amplitude ratio eSQQ between register value GC_Q and GC_I can be calculated as follows:

$$eSQQ = \frac{G\hat{C}\_Q}{G\hat{C}\_I}$$

The allowed range[3] for eSQQ is specified in Table 47.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Amplitude mismatch between I and Q | eSQQ | 0.5 | | 2 | | S_QQ[15:0] = $2^{15}$<br>Option Code -010 |
| | | 0.95 | | 1.05 | | S_QQ[15:0] = $2^{15}$<br>Option Code -000, -100 and -600 |

*Table 47: MLX90382ABA constraint on amplitude mismatch between I and Q*

[3] *If the specified amplitude mismatch range does not meet the requirements of your application, please contact Melexis.*

# 8 Package, IC handling and assembly

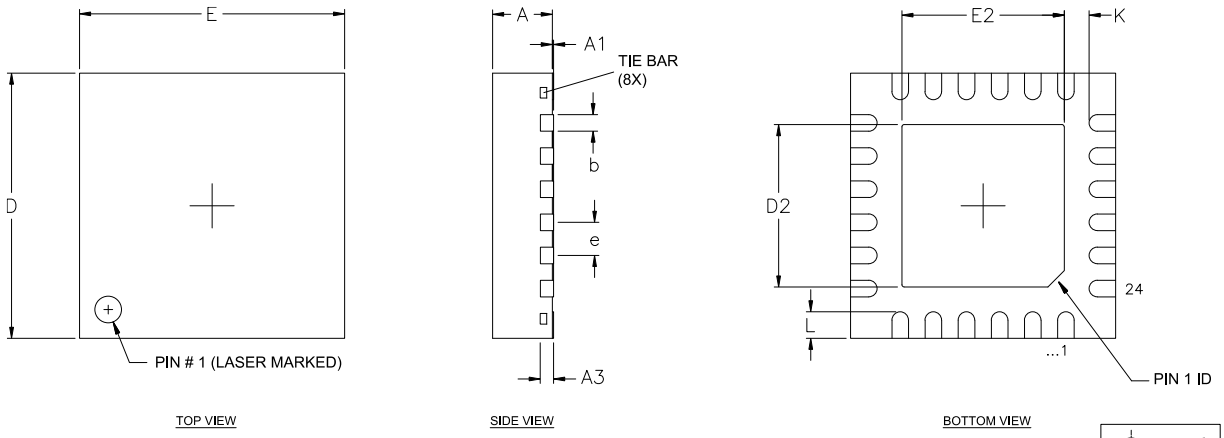
## 8.1 Package information

| Variant Code Marking | Definition (Option Code) |
|---|---|
| M | Rotary Mode Mid-Field (-000 and -010) |
| H | Rotary Mode High-Field (-100) |
| N | Stray Field Immune Rotary Mode (-600) |

*Table 48: Definition of the device variant marking on the package*

### 8.1.1 Package QFN-24 4x4

#### *8.1.1.1 Package QFN-24 dimensions*




NOTE :
1. EXPOSED TIE BAR SHOULD BE KEPT FREE FROM SOLDER.
2. (OPTIONAL) SIDE WALL IMMERSION TIN PLATING MIN 1um THICK.

| SYMBOL | ALL DIMENSION ARE IN MILLIMETERS | | |
|---|---|---|---|
| | MINIMUM | NOMINAL | MAXIMUM |
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| D | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 |
| D2 | 2.35 | 2.45 | 2.55 |
| E2 | 2.35 | 2.45 | 2.55 |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | --- | --- |
| b | 0.18 | 0.25 | 0.30 |
| e | | 0.50 BSC | |

*Figure 27: Package QFN-24 dimensions*

#### *8.1.1.2 Package QFN-24 pinout & marking*

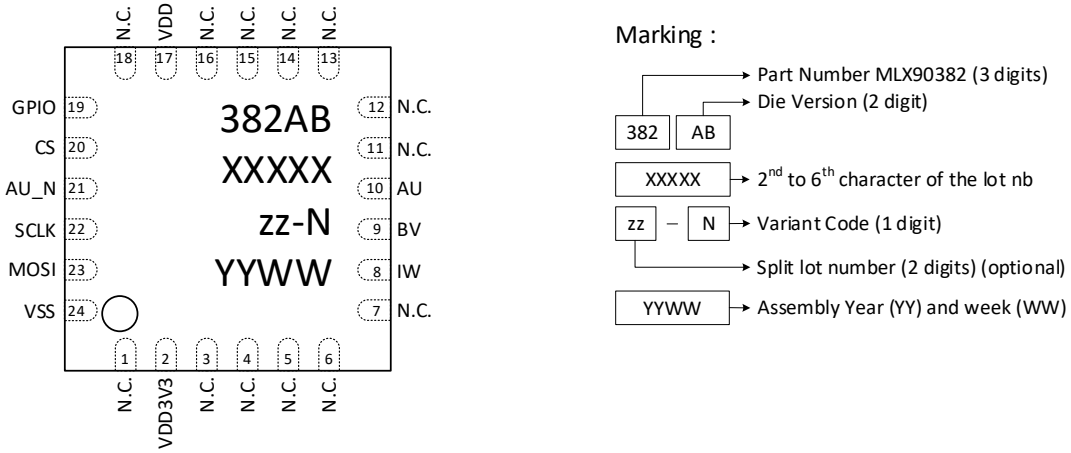
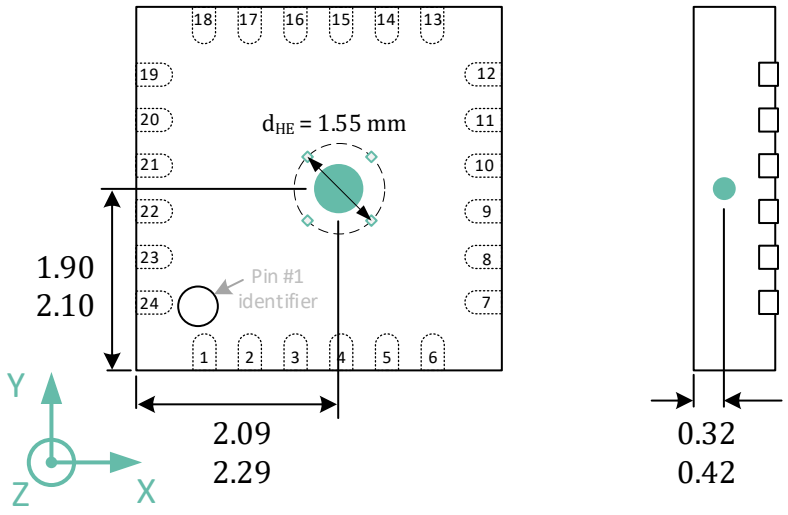



*Figure 28: Package QFN-24 pinout & marking*

#### *8.1.1.3 Package QFN-24 magnetic sweet-spot*

The location of the hall plates used for the stray field immune rotary mode are market as green rectangles.

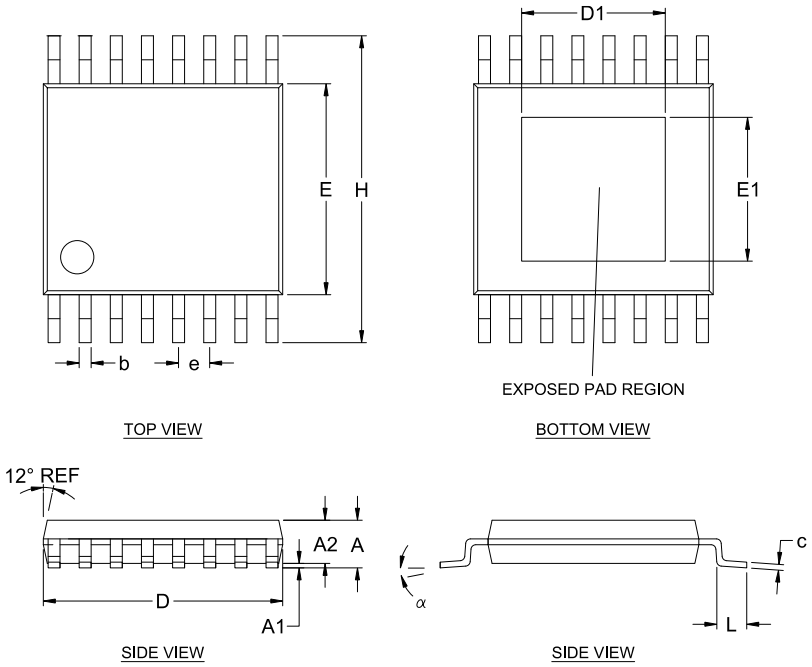



*Dimensions in "mm"*

*Figure 29: Package QFN-24 magnetic sweet-spot*

## 8.1.2 Package TSSOP-16_EP

### *8.1.2.1 Package TSSOP-16_EP dimensions*




| SYMBOL | MINIMUM | MAXIMUM |
|---|---|---|
| A | --- | 1.10 |
| A1 | 0.05 | 0.15 |
| A2 | 0.85 | 0.95 |
| D | 4.90 | 5.10 |
| E | 4.30 | 4.50 |
| D1 | 2.90 | 3.10 |
| E1 | 2.90 | 3.10 |
| H | 6.40 REF | |
| L | 0.50 | 0.75 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| e | 0.65 BSC | |
| α | 0° | 8° |

NOTE :
1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS OF MAX 0.15 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTERLEADS FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.08 mm.
5. LEAD COPLANARITY SHALL BE MAXIMUM 0.1 mm.

*Figure 30: Package TSSOP-16_EP dimensions*

### *8.1.2.2 Package TSSOP-16_EP pinout & marking*

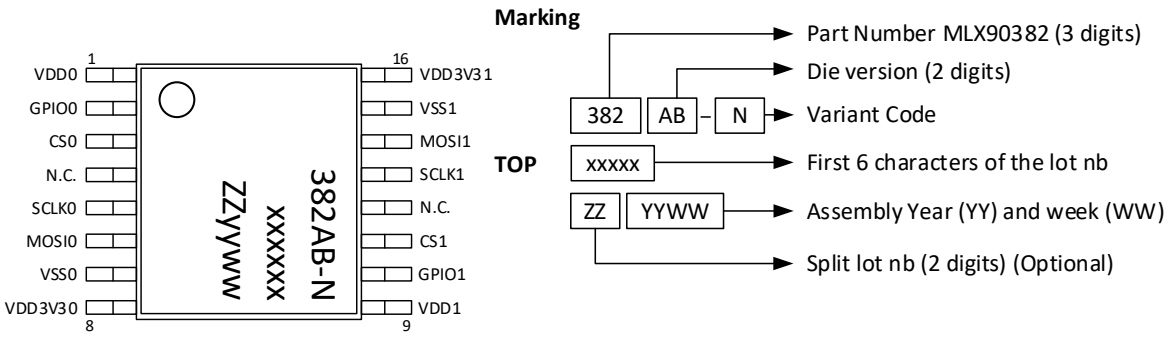



*Figure 31: Package TSSOP-16_EP pinout & marking*

#### *8.1.2.3 Package TSSOP-16_EP magnetic sweet spot*

The location of the hall plates used for the stray field immune rotary mode are market as green rectangles.

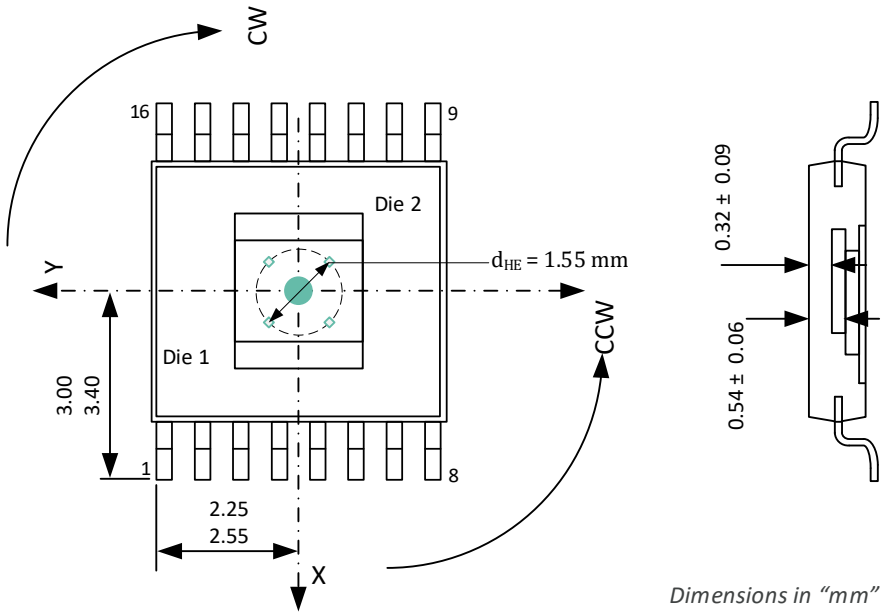



*Figure 32: Package TSSOP-16_EP magnetic sweet spot*

## 8.2 Storage and handling of plastic encapsulated ICs

Plastic encapsulated ICs shall be stored and handled according to their MSL categorization level (specified in the packing label) as per J-STD-033. Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). The component assembly shall be handled in EPA (Electrostatic Protected Area) as per ANSI S20.20 For more information refer to Melexis *Guidelines for storage and handling of plastic encapsulated ICs* [4]

## 8.3 Assembly of encapsulated ICs

For Surface Mounted Devices (SMD, as defined according to JEDEC norms), the only applicable soldering method is reflow.

For Through Hole Devices (THD), the applicable soldering methods are reflow, wave, selective wave and robot point-to-point. THD lead pre-forming (cutting and/or bending) is applicable under strict compliance with Melexis *Guidelines for lead forming of SIP Hall Sensors* [4].

Melexis products soldering on PCB should be conducted according to the requirements of IPC/JEDEC and J-STD-001. Solder quality acceptance should follow the requirements of IPC-A-610.

For PCB-less assembly refer to the relevant application notes [4] or contact Melexis.

Electrical resistance welding or laser welding can be applied to Melexis products in THD and specific PCB-less packages following the *Guidelines for welding of PCB-less devices*[4].

Environmental protection of customer assembly with Melexis products for harsh media application, is applicable by means of coating, potting or overmolding considering restrictions listed in the relevant application notes [4]

For other specific process, contact Melexis via www.melexis.com/technical-inquiry

[4] www.melexis.com/ic-handling-and-assembly

## 8.4 Environment and sustainability

Melexis is contributing to global environmental conservation by promoting non-hazardous solutions. For more information on our environmental policy and declarations (RoHS, REACH…) visit www.melexis.com/environmental-forms-and-declarations

# 9 User programmable items

The MLX90382 provides various programming options. It is designed and factory-programmed to require a minimal configuration setup. Both reading and writing operations of registers are supported via SPI. When configuring the registers, any unused bits must be set to "0", otherwise the NVRAM shadow register monitor causes triggering a safe state (see MLX90382 Safety Manuals).

## 9.1 MLX90382 Address Space

The MLX90382 address space is organized in read/writeable volatile DSP register and NVRAM register.

| Address - Range | | Description |
|---|---|---|
| 0x000 | 0x0FF | R/W volatile DSP register |
| 0x100 | 0x15A | Customer R/W NVRAM register |

*Table 49: MLX90382 address space organization*

## 9.2 Register Description

## 9.3 DSP Register

| Register | Address | Bit | R/W | Default | Description |
|---|---|---|---|---|---|
| **LIN_PHASE** | 0x03E | [15:0] | R/W | 0 | Angular value after linearization, resolution $360/2^{16}$ deg; Writable only with LOCK_PHASE = 1; Before delay compensation |
| **SPEED** | 0x040 | [15:0] | R/W | 0 | LSB of measured speed;<br>v[Hz] = signed(SPEED) / $2^{22}$ * $f_{ac}$/26;<br>v[rpm] = v[Hz] * 60; range ±6009,43 @ $f_{ac}$ = 20 MHz;<br>Writable only with LOCK_SPEED = 1; |
| **DRIFTC_PHASE** | 0x046 | [15:0] | R | 0 | Angular value after delay compensation and zero-point offset correction, resolution $360/2^{16}$ deg |
| **SC_PHASE** | 0x048 | [15:0] | R | 0 | Position value after signal conditioning |
| **GC_I** | 0x04A | [15:0] | R/W | 0 | Gain-compensated I component (Averaging result) |
| **GC_Q** | 0x04E | [15:0] | R/W | 0 | Gain-compensated Q component (Averaging result) |
| **SOFT_RESET** | 0x004 | [1] | R/W | 0 | 0: No request to reset hardware<br>1: Request to reset hardware (automatically cleared after reset) |
| **PWM_PCNT** | 0x0EA | [15:0] | R | 0 | PWM period counter<br>(PWM_PCNT_ON = 1) |
| **TEMP** | 0x03C | [11:0] | R | 0 | Temperature range [200:0.125:711.875] [K] |

*Table 50: DSP register*

## 9.4 NVRAM Register

### 9.4.1 Magnetic Sensing Mode Configuration

| Register | Address | Bit | R/W | Default | Description |
|---|---|---|---|---|---|
| **SENSING_MODE** | 0x100 | [2:0] | R/W | 0 | Magnetic sensing mode:<br>Option Code -000:<br>0: X-Y (default), 1: X-Zy, 2: Y-Zx<br>Option Code -100:<br>0: X-Y (default)<br>Option Code -010:<br>1: X-Zy (default), 2: Y-Zx<br>Option Code -600:<br>0: X-Y (default) |

*Table 51: Magnetic sensing mode configuration register*

### 9.4.2 Interface Configuration

| Register | Address | Bit | R/W | Default | Description |
|---|---|---|---|---|---|
| **GPIO_IF** | 0x100 | [4:3] | R/W | 1 | GPIO protocol:<br>0: PWM/Differential ABI or UVW;<br>1: SSI; 2: SPI bus mode |
| **ABI_IF** | | 5 | R/W | 1 | ABI / UVW protocol:<br>0: UVW; 1: ABI |
| **GPIO_CFG** | | [10:6] | R/W | 28 | GPIO output driver strength:<br>GPIO_CFG[8:6]:<br>Do not change or overrides factory trimming for **5V mode** only. Use max. driving strength for **3.3V mode** only.<br>GPIO Output driver-mode:<br>GPIO_CFG[10:9]:<br>0: off,<br>1: open-drain p-MOS,<br>2: open-drain n-MOS<br>3: push-pull |
| **ABI_CFG** | | [15:11] | R/W | 28 | ABI output driver strength:<br>ABI_CFG[13:11]<br>Do not change or Overrides factory trimming for **5V mode** only. Use max. driving strength for **3.3V mode** only.<br>ABI Output driver-mode:<br>ABI_CFG[15:14]<br>0: off,<br>1: open-drain p-MOS,<br>2: open-drain n-MOS<br>3: push-pull |
| **ABI_LOG2N** | 0x104 | [3:0] | R/W | 3 | ABI number of counts per revolution with: 4 * 2^ABI_LOG2N |
| **UVW_PP** | | [8:4] | R/W | 0 | UVW pole pairs |
| **ABIUVW_DIR** | | 9 | R/W | 0 | ABI / UVW rotation direction |
| **ABIUVW_HYS** | | [13:10] | R/W | 6 | ABI / UVW hysteresis:<br>$\pm floor(2^{(ABIUVW\_HYS-1)})$ |
| **PWM_INV** | | 14 | R/W | 0 | PWM waveform inversion |

| Register | Address | Bit | R/W | Default | Description |
|---|---|---|---|---|---|
| **PWM_PCNT_ON** | | 15 | R/W | 0 | PWM period counter (PWM_PCNT),<br>0: period counter off,<br>1: PWM counter running despite GPIO_IF setting |
| **PWM_PERIOD** | 0x12E | [15:0] | R/W | 4095 | PWM period |
| **PWM_DC_OFS** | 0x148 | [8:0] | R/W | 0 | PWM Duty Cycle offset trimming |
| **SPI_FADDR0** | 0x130 | [7:0] | R/W | 0 | SPI FR Address 0 |
| **SPI_FADDR1** | | [15:8] | R/W | 0 | SPI FR Address 1 |
| **SPI_FADDR2** | 0x132 | [7:0] | R/W | 0 | SPI FR Address 2 |
| **SPI_FADDR3** | | [15:8] | R/W | 0 | SPI FR Address 3 |
| **SPI_FRFS** | 0x134 | [3:0] | R/W | 10 | SPI FR frame start pattern |
| **SPI_FRCRCEN** | | [5] | R/W | 1 | SPI FR CRC enable |
| **SPI_FRFSEN** | | [4] | R/W | 1 | SPI FR frame start enable |
| **SPI_FRINV** | | [9:6] | R/W | 0 | SPI FR data inversion |
| **SPI_MODE** | | [11:10] | R/W | 1 | SPI Mode selection<br>Mode / SPI_MODE[11:10] (CPOL, CPHA)<br>0: 0, 0<br>1: 0, 1<br>2: 1, 0<br>3: 1, 1 |
| **SPI_DMY** | | [13:12] | R/W | 0 | SPI output optional word alignment<br>SPI_DMY[13] = 1: Add additional dummy byte transfer after byte 2 in RR mode<br>SPI_DMY[12] = 1: Add additional dummy byte transfer after byte 2 in FR mode |
| **SPI_SFRL** | 0x136 | [7:0] | R/W | 0 | SPI super frame length |
| **SPI_SFRDLY** | | [15:8] | R/W | 0 | SPI FR delay within super frame |
| **SPI_CPTLT** | 0x138 | [2:0] | R/W | 0 | SPI capture lead time synchronous (SPI_CPTLT + 1) * TSCLK before the DATA(FADDR0)[15:8] byte |
| **SPI_SFR_SCPT** | | 3 | R/W | 1 | Synchronize the angle capture time point on all slaves to the position of the DATA(FADDR0)[15:8] byte with SPI_SFRDLY = 0 |
| **SPI_DBNC_CS** | | [7:4] | R/W | 0 | SPI CS debounce filter<br>$\tau_{CS}$ = SPI_DBNC_CS*2/$f_{RCO}$ |
| **SPI_DBNC** | | [11:8] | R/W | 0 | SPI SCLK/MOSI debounce filter<br>$\tau_{SCLK/MOSI}$ = SPI_DBNC/$f_{RCO}$ |
| **SSI_PARPOS** | 0x13A | [3:0] | R/W | 0 | SSI parity bit position for odd parity:<br>≤ 8: parity of angle[15:SSI_PARPOS+1] transmitted at bit position SSI_PARPOS<br>> 8: no parity bit - SSI data: angle[15:0] |
| **SSI_TM** | | [12:5] | R/W | 0 | SSI timeout, $T_M$ = (SSI_TM+1)*8/$f_{ac}$ |

| Register | Address | Bit | R/W | Default | Description |
|---|---|---|---|---|---|
| **SSI_CPT** | | 14 | R/W | 1 | In SSI mode, the DSP output shall be sampled at rate $f_{ac}$ depending on SSI_CPT (CUS, default: 0) as follows:<br>SSI_CPT = 0: falling edge on SCLK after start-up and falling edge auf pause pulse ($T_P$)<br>SSI_CPT = 1: $T_M$ after rising edge of pause pulse ($T_P$) |
| **PHY_RC_EN** | 0x13C | [2:0] | R/W | 0 | EMC RC filter enable:<br>Bit[0]: pin CS<br>Bit[1]: pin IW (QFN-24)/pin MOSI (TSSOP-16_EP)<br>Bit[2]: pin BV (QFN-24)/pin SCLK (TSSOP-16_EP) |

*Table 52: Interface configuration register*

### 9.4.3 Signal Conditioning and Processing

| Register | Address | Bit | R/W | Default | Description |
|---|---|---|---|---|---|
| **AGC_GAIN_MIN** | 0x108 | [5:0] | R/W | 0 | AGC minimum gain, range [0..47] |
| **AGC_GAIN_MAX** | | [11:6] | R/W | 47 | AGC maximum gain, range [0..47] |
| **AGC_GAIN** | 0x038 | [5:0] | R | 23 | Read current AGC gain setting |
| **PEQ_GAIN** | 0x10A | [2:0] | R/W | 0 | Linearization gain. If > 0, phase offsets per reference point angle are POFSxx[15:0] = signed(PEQxx) * $2^{(PEQ\_GAIN-1)}$<br>, else 0 |
| **PEQ00** | 0x10C | [7:0] | R/W | 0 | Phase Equalizer value at 0/16 * 360 deg |
| **PEQ01** | | [15:8] | R/W | 0 | Phase Equalizer value at 1/16 * 360 deg |
| **PEQ02** | 0x10E | [7:0] | R/W | 0 | Phase Equalizer value at 2/16 * 360 deg |
| **PEQ03** | | [15:8] | R/W | 0 | Phase Equalizer value at 3/16 * 360 deg |
| **PEQ04** | 0x110 | [7:0] | R/W | 0 | Phase Equalizer value at 4/16 * 360 deg |
| **PEQ05** | | [15:8] | R/W | 0 | Phase Equalizer value at 5/16 * 360 deg |
| **PEQ06** | 0x112 | [7:0] | R/W | 0 | Phase Equalizer value at 6/16 * 360 deg |
| **PEQ07** | | [15:8] | R/W | 0 | Phase Equalizer value at 7/16 * 360 deg |
| **PEQ08** | 0x114 | [7:0] | R/W | 0 | Phase Equalizer value at 8/16 * 360 deg |
| **PEQ09** | | [15:8] | R/W | 0 | Phase Equalizer value at 9/16 * 360 deg |
| **PEQ10** | 0x116 | [7:0] | R/W | 0 | Phase Equalizer value at 10/16 * 360 deg |
| **PEQ11** | | [15:8] | R/W | 0 | Phase Equalizer value at 11/16 * 360 deg |
| **PEQ12** | 0x118 | [7:0] | R/W | 0 | Phase Equalizer value at 12/16 * 360 deg |
| **PEQ13** | | [15:8] | R/W | 0 | Phase Equalizer value at 13/16 * 360 deg |
| **PEQ14** | 0x11A | [7:0] | R/W | 0 | Phase Equalizer value at 14/16 * 360 deg |
| **PEQ15** | | [15:8] | R/W | 0 | Phase Equalizer value at 15/16 * 360 deg |
| **S_IQ** | 0x11C | [15:0] | R/W | 0 | Relative cross-sensitivity from in-phase to quadrature phase component, range [$-2^{15}$,$+2^{15}$); overrides factory trimming, if non-zero |
| **S_QQ** | 0x11E | [15:0] | R/W | 32768 | Relative sensitivity for quadrature component, range [0,$2^{16}$-1); overrides factory trimming if not $2^{15}$. |

| Register | Address | Bit | R/W | Default | Description |
|---|---|---|---|---|---|
| **PHASE_OFS** | 0x120 | [15:0] | R/W | 0 | Phase/Angle offset before signal conditioning, resolution $360/2^{16}$ deg (signed 2th-complement) |
| **SC_X1** | 0x122 | [15:0] | R/W | 0 | Signal conditioning: X1, input range low |
| **SC_X2** | 0x124 | [15:0] | R/W | 0 | Signal conditioning: X2, input range high |
| **SC_Y1** | 0x126 | [15:0] | R/W | 1 | Signal conditioning: Y1, output range low |
| **SC_Y2** | 0x128 | [15:0] | R/W | 32765 | Signal conditioning: Y2, output range high |
| **SC_YE** | 0x12A | [15:0] | R/W | 32766 | Signal conditioning: output fault band level |
| **DELAY_CUS** | 0x144 | [7:0] | R/W | 0 | Customer processing delay, range [0:255] * 26/64 / $f_{RCO}$ |
| **DSP_IQNEG** | 0x146 | [1:0] | R/W | 0 | I/Q sign inversion:<br>Bit[0]: 0: GC_I, 1: -GC_I<br>Bit[1]: 0: GC_Q, 1: -GC_Q |
| **DSP_GC_AVG** | | [4:2] | R/W | 0 | GC averaging control:<br>0: Averaging off,<br>1…6: sum(k = 1..4^DSP_GC_AVG, gc_x/4^DSP_GC_AVG)<br>7: sum(k = 1..8, gc_x/8) |
| **DSP_DRIFTC_DIS** | | 5 | R/W | 0 | 1: Disable delay compensation |
| **DSP_LFC_LO** | | [10:8] | R/W | 3 | Lowest DSP loop filter bandwidth; adaptive loop filter enabled, if DSP_LFC_LO < DSP_LFC_HI |
| **DSP_LFC_HI** | | [13:11] | R/W | 3 | Upper DSP loop filter bandwidth |
| **DSP_SROS** | | [15:14] | R/W | 2 | Phase tracking step response overshoot |

*Table 53: Signal conditioning and processing register*

### 9.4.4 Miscellaneous

| Register | Address | Bit | R/W | Default | Description |
|---|---|---|---|---|---|
| **CUS_CRC** | 0x15A | [15:0] | R/W | 0 | CUS area checksum (CRC16 CCITT) |
| **ANA_VERSION** | 0x0EE | [7:0] | R | 0 | Analog Version |
| **DIG_VERSION_L** | | [15:8] | R | 0 | Digital Version (8 LSB) |
| **DIG_VERSION_H** | 0x0F0 | [15:0] | R | 0 | Digital Version (16 MSB) |
| **USER_ID0** | 0x13E | [7:0] | R/W | 0 | Reserved for customers for traceability |
| **USER_ID1** | | [15:8] | R/W | 0 | Reserved for customers for traceability |
| **USER_ID2** | 0x140 | [7:0] | R/W | 0 | Reserved for customers for traceability |
| **USER_ID3** | | [15:8] | R/W | 0 | Reserved for customers for traceability |
| **USER_ID4** | 0x142 | [7:0] | R/W | 0 | Reserved for customers for traceability |
| **USER_ID5** | | [15:8] | R/W | N/A | Reserved for customers for traceability |

*Table 54: Miscellaneous register*

# 10 Glossary of terms & references

## 10.1 Glossary

| Term | Description |
|---|---|
| ADC | Analog-to-Digital Converter |
| ASIL | Automotive Safety Integrity Level |
| BLCD | Brushless DC Electric Motor |
| CDM | Charged Device Mode |
| CRC | Cyclic Redundancy Check |
| CS | Chip Select |
| CPHA | Clock Phase |
| CPOL | Clock Polarity |
| dBz mode | Stray Field Immune Mode |
| DSP | Digital Signal Processing |
| ECU | Electronic Control Unit |
| EMC | Electro-Magnetic Compatibility |
| EoL | End of Line |
| ESD | Electrostatic discharge |
| FR | Frame Read |
| HBM | Human Body Model |
| IMC | Integrated Magnetic Concentrator |
| INL / DNL | Integral Non-Linearity / Differential Non-Linearity |
| LFC | Low-pass Filter Constant |
| MISO | Master Input Slave Output |
| MOSI | Master Output Slave Input |
| MSB | Most Significant Bit |
| MUX | Multiplexer |
| NC | Not Connected |
| NVRAM | Non-Volatile RAM |
| LSB/MSB | Least Significant Bit / Most Significant Bit |
| OV/UV | Overvoltage / Undervoltage |
| OS | Overshoot |
| PWM | Pulse Width Modulation |
| RPM | Revolutions Per Minute |
| RAM | Random-Access Memory |
| RR | Register Read |
| RW | Register Write |
| SCLK | Serial Clock |
| SFR | Super-Frame Read |
| SPI | Serial Peripheral Interface |
| SSI | Synchronous Serial Interface |
| TDMA | Time Division Multiple Access |
| Tesla (T) | SI derived unit for the magnetic flux density (Vs/m2) |

## 10.2 References

Following documents are referred to in this document:

[1] Stress test qualification standard JEDEC47L qualified
[2] Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices, IPC J-STD-033
[3] MLX90382 Safety Manual (single die)
[4] MLX90382 Safety Manual addendum for IEC61508 compliance
[5] ANSI/ESD S20.20-2021: Protection of Electrical and Electronic Parts
[6] IEC61508

The descriptions in this document overrule the descriptions in the referred documents.

## 10.3 List of Tables

## 10.4 List of Figures

## 11 Revision history

| Revision | Date | Change history |
|---|---|---|
| 1.00 | 21-Nov-24 | Official datasheet release |
| 2.00 | 27-Nov-24 | Updated minimum PWM frequency. Updated available Sensing Modes for Ordering-Code MLX90382LLW-ABA-100-RE. |
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