Melexis

INSPIRED ENGINEERING

APPLICATION NOTE

Guidelines for potting of plastic encapsulated ICs (rev 1.0)

February 2021

Advanced Customer Solutions

Guidelines for potting of plastic encapsulated ICs

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1. Scope

Environmental and mechanical protection for Melexis products

Melexis products are plastic encapsulated devices and as such are considered non-hermetic packages: therefore they shall always be protected by potting or conformal coating in harsh media applications. Potting consists on dispensing a significant volume of adhesive in a housing. Conformal coating is a thin layer (applied by spray, brush or dipping) on top of the PCB or component surface

Environmental and mechanical protection

Potting

- **Role 1:** Environmental and chemical protection
- **Role 2:** FOD (Foreign Object Debris) protection
- **Role 3:** Mechanical shock and vibration protection

Conformal coating

- **Role 1:** Environmental and chemical protection
- **Role 2:** FOD (Foreign Object Debris) protection

Apply potting to achieve mechanical shock and vibration protection

For pressure sensor cavity packages, potting is also applied for hermetic sealing

1. Scope

Basic potting flow for PCB and PCB-less applications

Application of potting is a frequently applied process and consists of the following steps:

1. **Dispensing**: The liquid polymer is dispensed into the plastic housing and component inside with accurate control of position and volume.
2. **Curing**: The liquid polymer is cross-linked either by humidity (at room temperature), UV light and/or heat until it completely solidifies.
3. **Inspection**: Automatic Optical Inspection (AOI) checks that the proper volume has been dispensed, as well as any surface defects and potting voids of the assembly. Mechanical hardness test by force/distance measurement on top of the potting surface maybe applied to verify cure completion.

Dispensing/curing might be done in two steps to help outgassing when the potting volume and thickness is high.

Storage and handling of Melexis devices at customer side should follow guidelines in J-STD-033 *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*. Key parameters are printed on the label attached to the product packing. Refer to *Guidelines for storage and handling of plastic encapsulated ICs* on Melexis website for details.

Guidelines for potting of plastic encapsulated ICs

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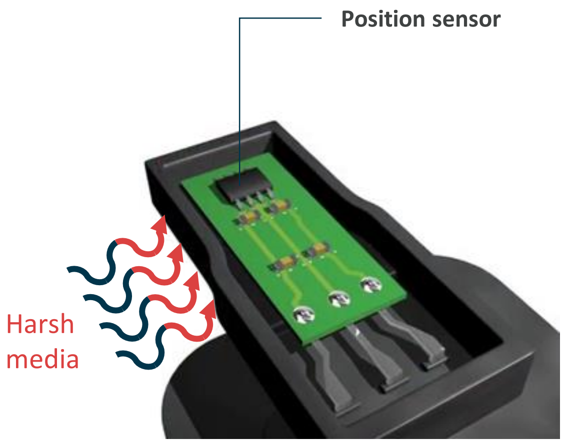
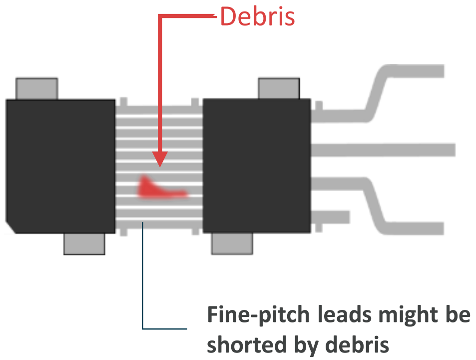
2. Potting selection

Risks to be eliminated by potting



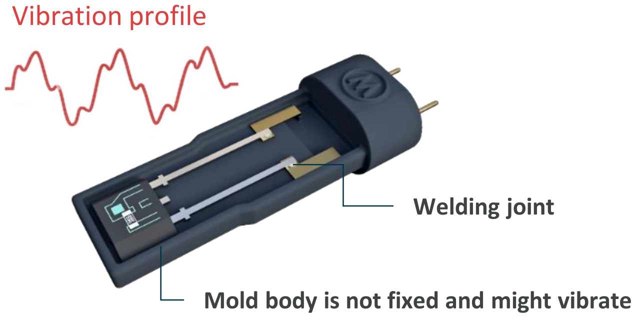
1: Environmental and chemical risk

Plastic encapsulated packages are non-hermetic and can absorb liquid/vapour phase substances (moisture and chemicals)



2: FOD risk

Debris from nearby sources might fall on the sensor. This is specially critical for DMP packages to avoid a short in the fine pitch leads between the two molds.



3: Mechanical shock and vibration risk

In PCB-less applications there is no PCB where the components are soldered to: the component leads between the welding joint and the mold body are prone to vibrate and might get damage.

2. Potting selection

General criteria for potting material selection

Criteria	
	Working temperature – It should have stable physical characteristics in the whole temperature range of the intended application.
	Adhesion - High adhesion to thermoplastic and thermoset polymers in the working temperature range
	Coefficient of Thermal Expansion (CTE) - CTE close to the CTE of the plastic housing
	Hardness- Sufficient hardness to withstand shock and vibration stress characteristic of the application (elastic materials do not have enough hardness)
	Water absorption rate – Low water absorption rate
	Chemical resistance - Excellent resistance to intended harsh media (transmission oil, fuel, brake fluid…..in liquid and vapor phase)
	Viscosity - Adequate (low) viscosity to fill complex cavity shape without voids
	Cure profile - Guaranteeing full cure and out-gassing; complex or deep cavities may need to be potted in 2 steps to allow outgassing

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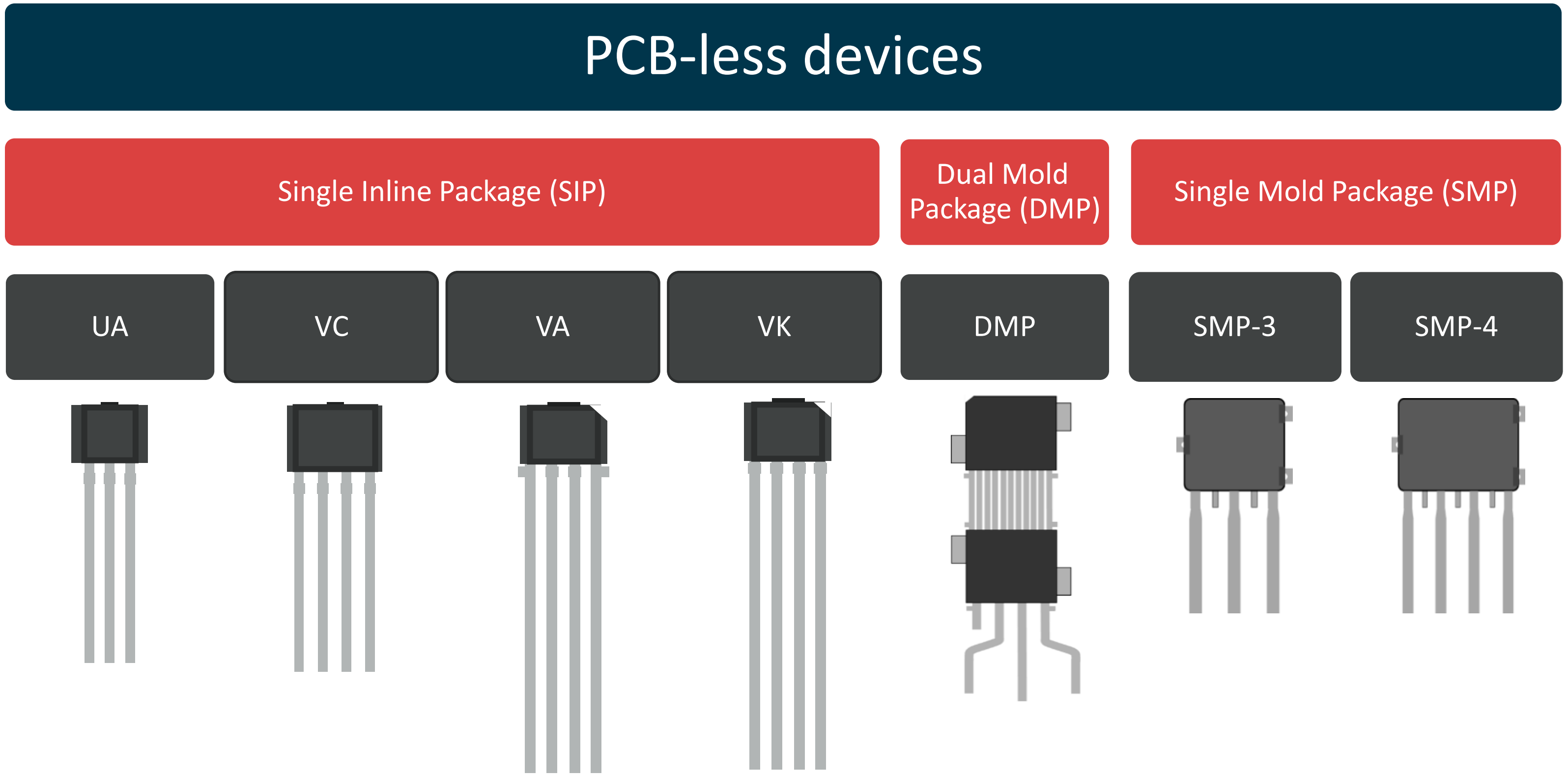
3. Potting in PCB-less applications

Family of Melexis packages for PCB-less applications



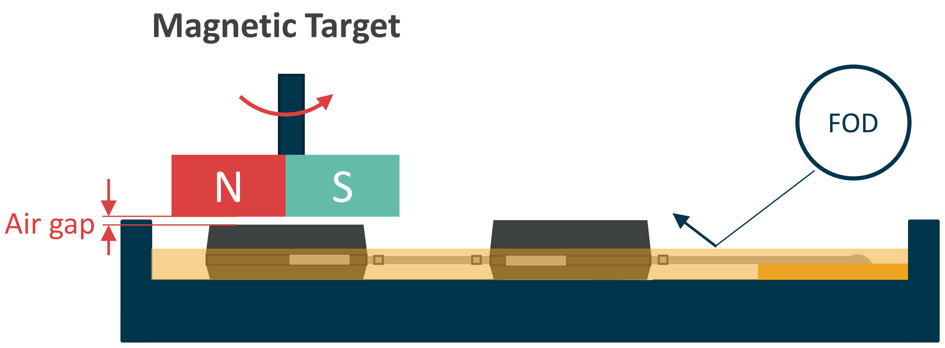
Refer to Annex I for the different abbreviations

3. Potting in PCB-less applications

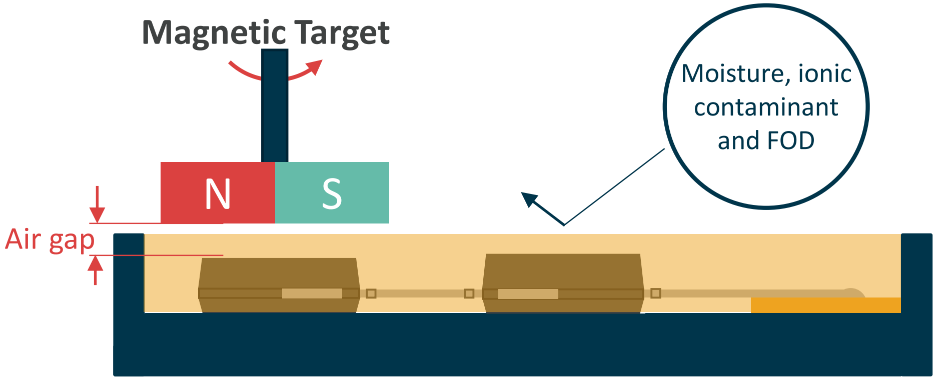
Design concepts for PCB-less

There are two main concepts for potting:

- Shallow potting: It can be used when the distance of the Hall plate to the target (usually a magnet) is critical and there is no harsh media. In this scenario the Hall sensor mold is exposed and the air gap is kept to a minimum. Shallow potting protects from FOD and mechanical shock and vibration.
- Deep potting: It should be used when harsh media and mechanical protection are required. In this scenario the whole component is covered and the potting acts as a harsh media barrier and mechanical fixation.



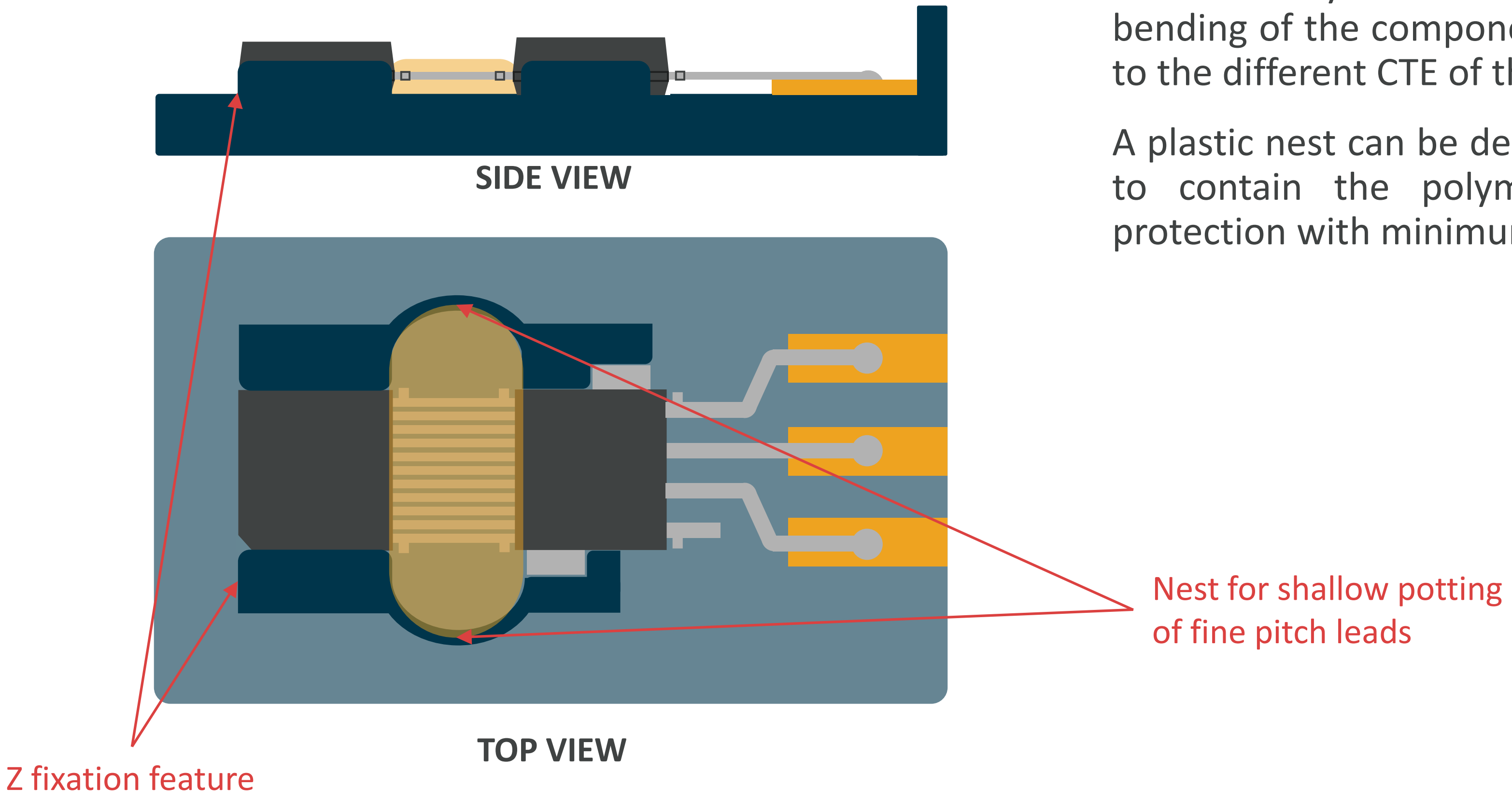
Shallow potting:
The Hall sensor mold is exposed when the distance to the target is critical and mechanical protection is needed



Deep potting:
The whole component is covered when the environmental and mechanical protection are critical

3. Potting in PCB-less applications

Local potting for FOD protection

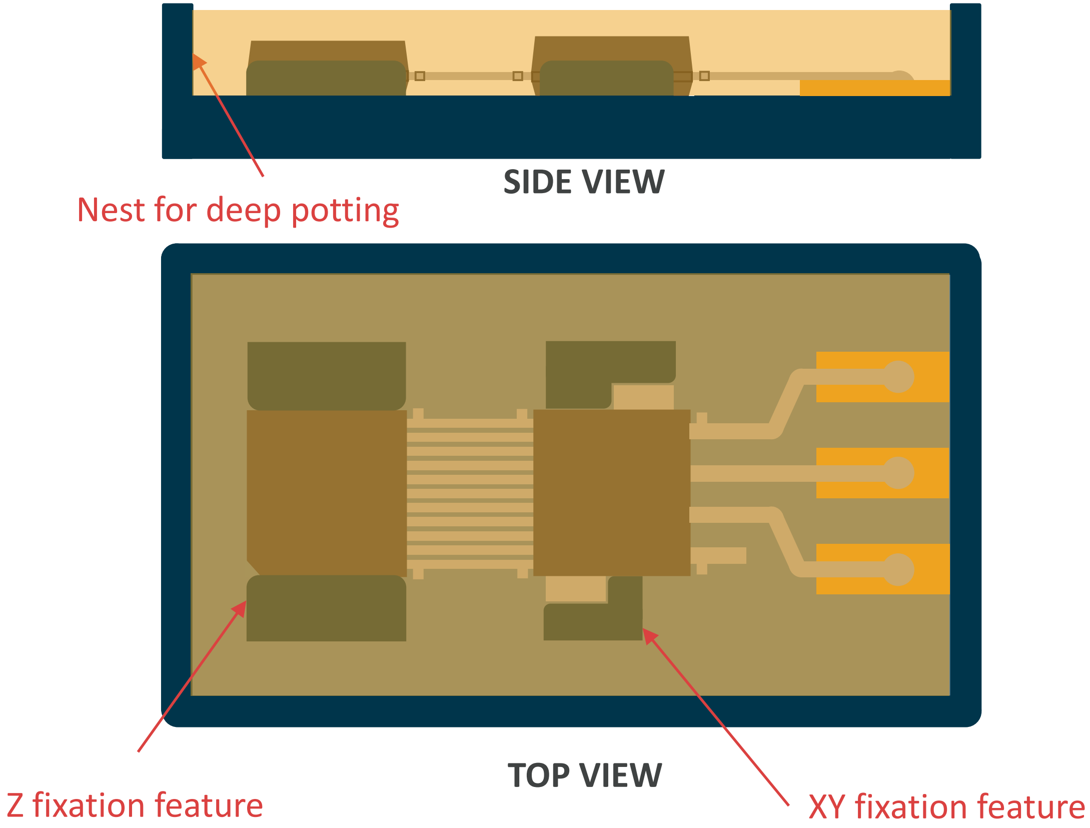


Z fixation by hot riveting is recommended to reduce bending of the component during thermal excursions due to the different CTE of the IC and the potting material.

A plastic nest can be designed around the fine pitch leads to contain the polymer material and achieve FOD protection with minimum material use

3. Potting in PCB-less applications

Full potting, protecting against harsh media, FOD and vibration/shock



Z-fixation before potting is a must to avoid an air gap between the IC mold and housing surface what may not be filled by potting.

The nest for deep potting is all around the sensor and should be high enough so that the polymer covers completely the IC.

For shallow potting, the IC active surface is exposed

Adhesion between the potting and plastic housing can be improved by roughening the surface or by laser grooving

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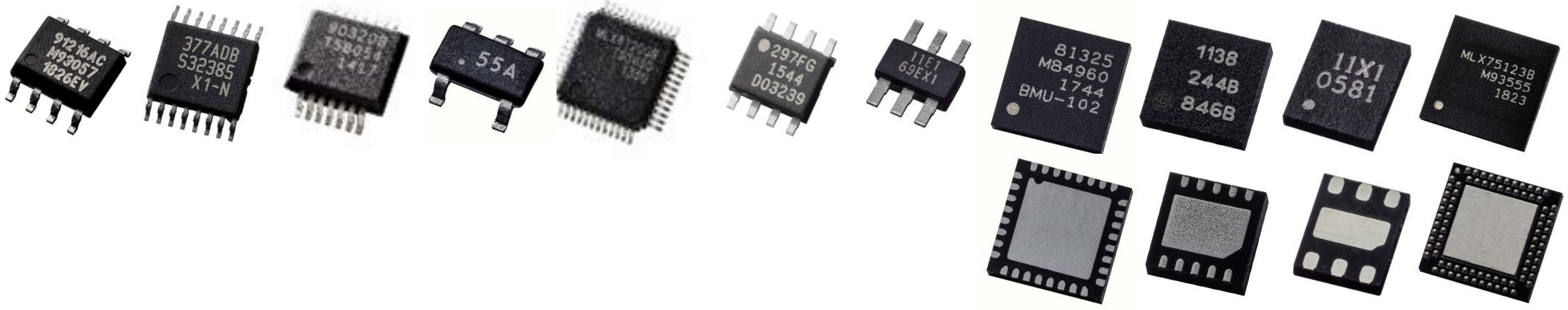
4. Potting in PCB applications

Family of Melexis packages for PCBA applications

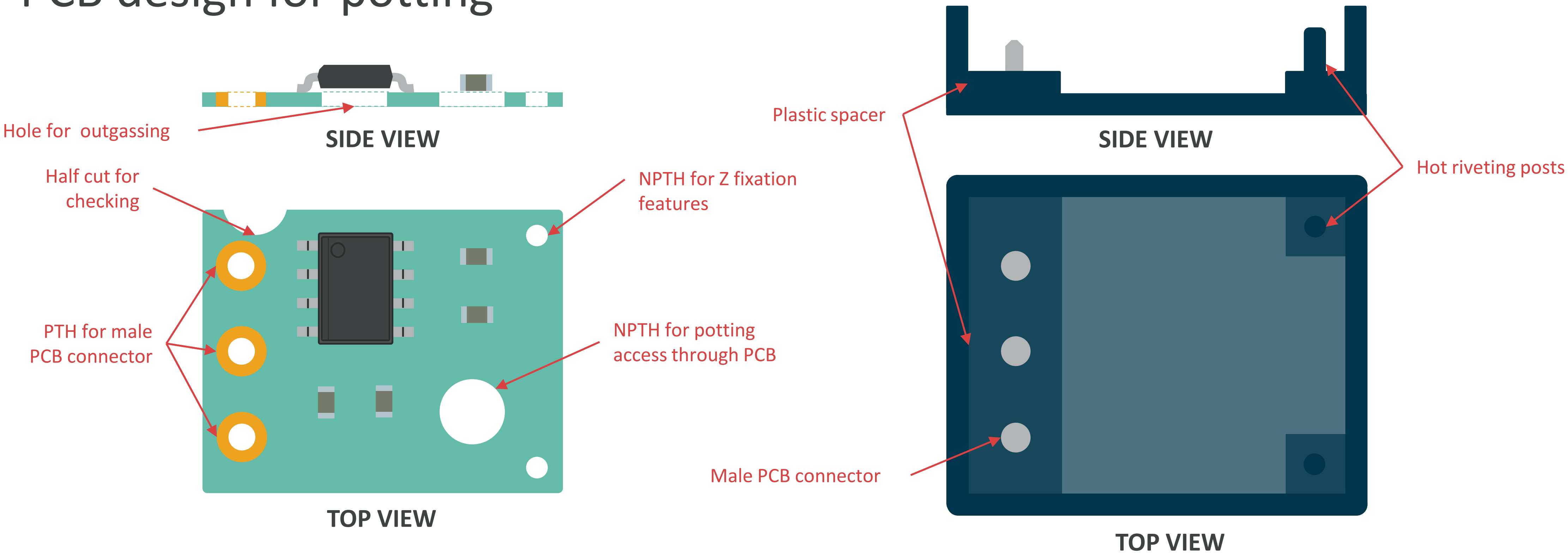
Surface Mount Devices (SMD)										
Gull wing					Straight leads		Bottom Terminated Component (BTC)			
SOIC	TSSOP	SSOP	SOT	QFP	SOIC	SOT	QFN	DFN	UTDFN	BGA



Refer to Annex I for the different abbreviations

4. Potting in PCB applications

PCB design for potting



The process steps for potting are:

1. PCB insertion into housing
2. Connector pin soldering and hot riveting
3. Potting

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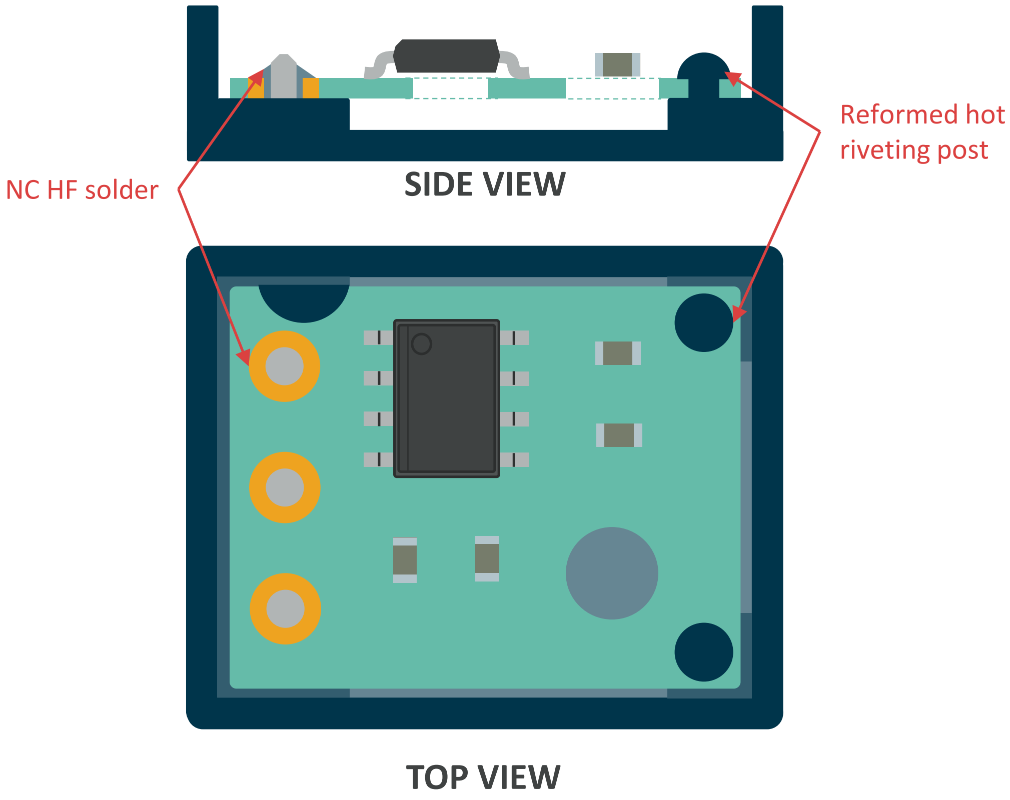
4. Potting in PCB applications

PCB preparation for potting



During potting, solder flux residual on PCB surfaces will be trapped in the interface between the PCB and the potting material. To avoid corrosion risk, it is recommended to use a no-clean (NC) halogen-free (HF) solder paste for reflow soldering of the PCB. Alternatively, sufficient washing might be applied to guarantee a clean surface without contaminants. Refer to *Guidelines for Surface Mount Technology (SMT) soldering* in Melexis website for more information

For connector soldering, it is recommended to use a no-clean halogen-free solder wire since washing is not possible.

Reflow soldering of component

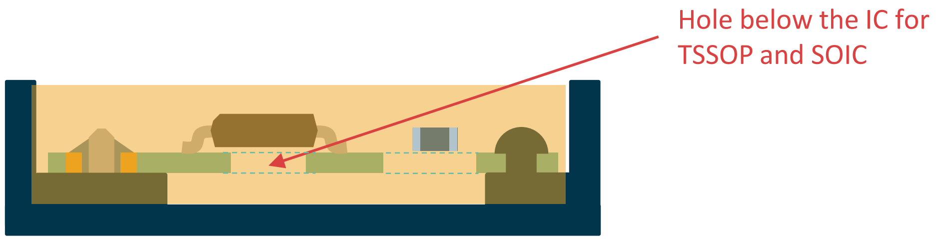
- Option 1: NC HF solder paste
- Option 2: PCB washing

Robot soldering of connector

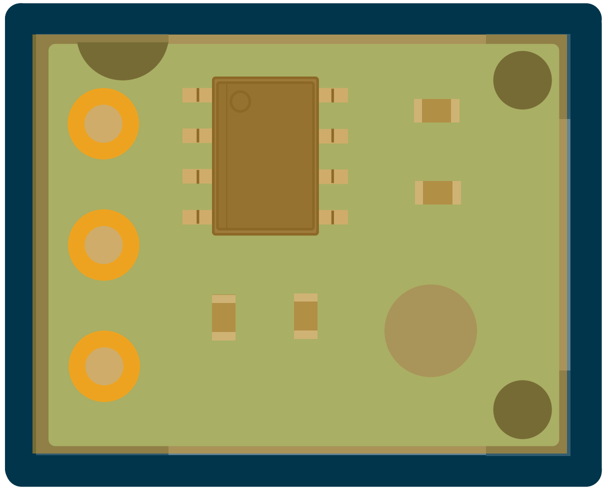
- NC HF solder wire

4. Potting in PCB applications

Plastic housing design for potting



SIDE VIEW



TOP VIEW

To completely fill the space under the PCB a non-plated through hole (NPTH) for dispensing should be designed on the PCB

Z fixation in the side opposite to the connector is recommended to reduce bending of the PCB during thermal excursions due to the different CTE of the PCB and the potting material. This fixation might be achieved by PCB solder via to a connector dummy pins or hot riveting to the housing posts.

For low stand-off (100 um) TSSOP devices, a hole in the PCB right below the IC help avoiding trapped air between the mold body of the IC and the PCB surface. A hole is not needed for QFN and SOT packages due to the small outline of the mold package

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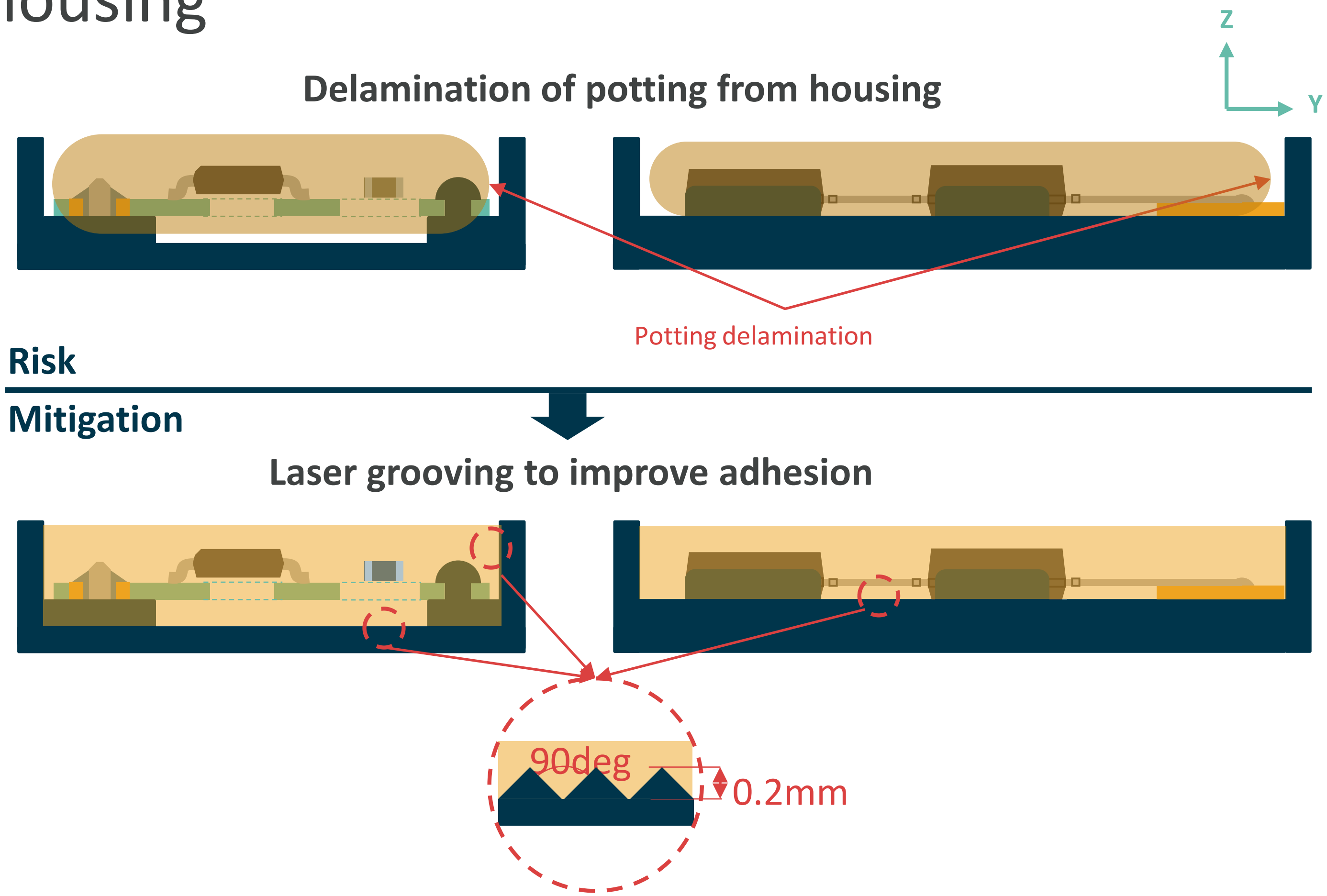
5. Known potential failures modes of potting

Failure mode 1: Potting delamination from housing due to the CTE mismatch of potting and housing

Risk: If the CTEs of both materials are too different, potting may detach from the housing wall/bottom during thermal excursions. As a result, both harsh media and vibration protection functions of potting are jeopardized.

Detection: Sensitivity to potting delamination should be tested by thermal cycling: for example, 500TC with temperature -55/+150C with 30min or 15 min dwell time, air to air (elevator).

Mitigation: Adhesion strength during thermal excursions can be improved if the housing surface is roughened - typically by mold tool surface design or by extra laser grooving.



5. Known potential failures modes of potting

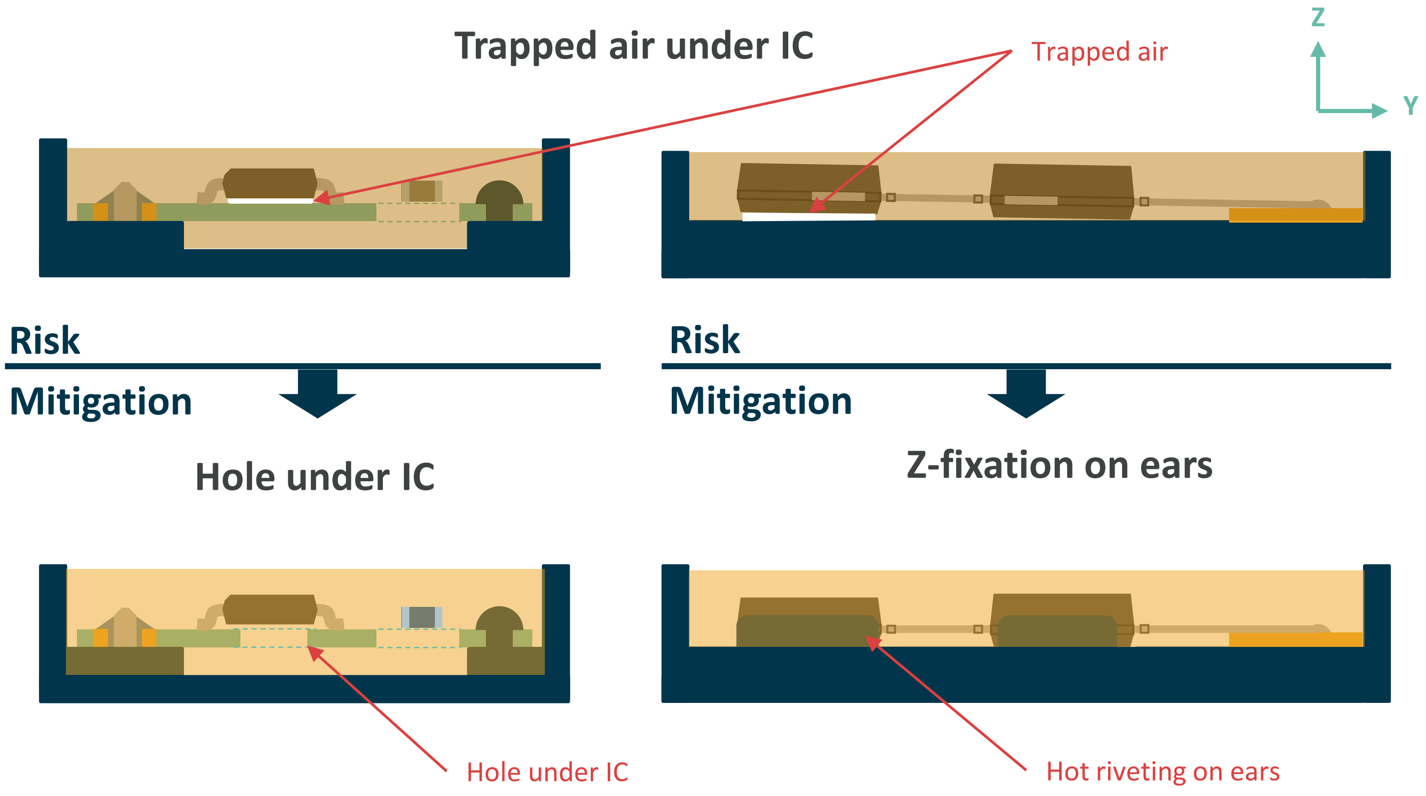
Failure mode 2: Stress on IC due to air trapped under the IC

Risk: Air trapped under the IC might create localized stress on the mold body during thermal excursions due to the different CTE of the trapped air compared to the potting.

Detection: Output sesnitivity/offset drift, loss of function

Mitigation:

- For PCB assemblies: A hole under the IC to help potting reach below the mold body – this is only needed for low stand-off devices (<100 um)
- For PCB-less assemblies: Z fixation of the IC to guarantee contact between the mold body and the plastic housing



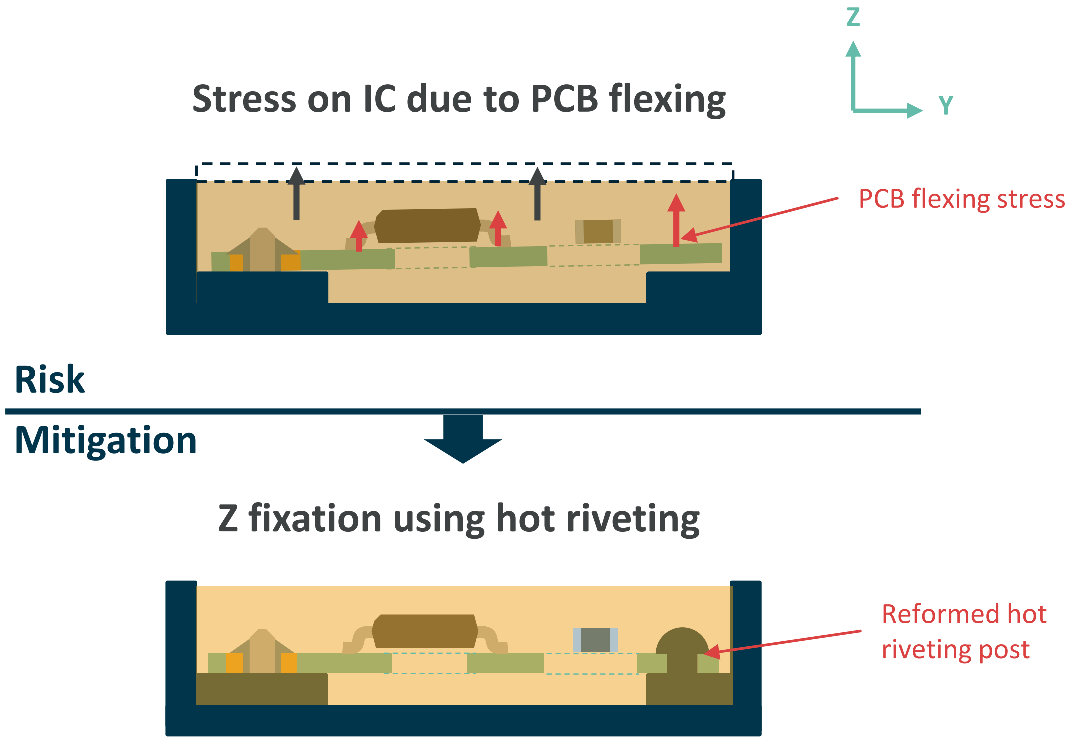
5. Known potential failures modes of potting

Failure mode 3: Stress on IC due to PCB flexing by potting thermal expansion

Risk: During thermal excursions, the potting material will expand to the open space (Z in the sketch). If there is not Z fixation of the PCB to the plastic housing, the PCB might flex, which will create stress on the IC.

Detection: Output sensitivity drift, offset drift or loss of function

Mitigation: Two side fixation of the PCB to the plastic housing, either by dummy soldered connectors or hot riveting posts.



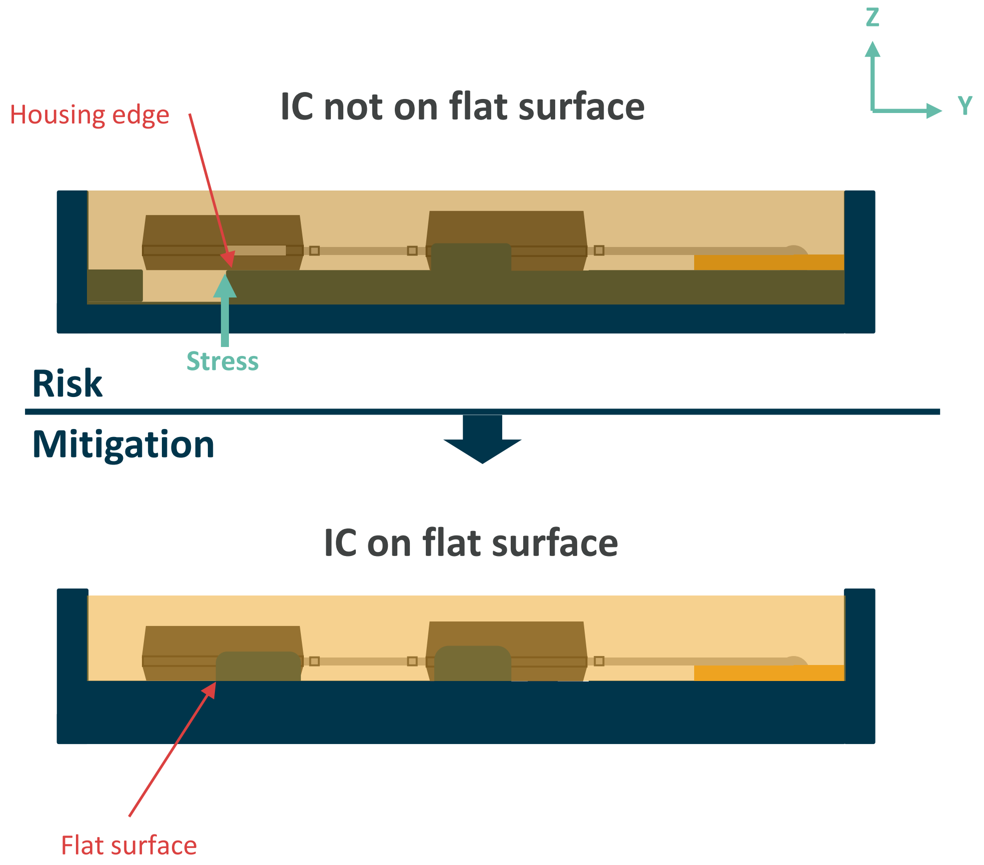
5. Known potential failures modes of potting

Failure mode 4: IC not on a flat surface, housing edge acting as a stress factor

Risk: The plastic housing edge might act as a stress factor on the mold body of the IC (both Hall mold and capacitor mold). This might lead to internal structural damage.

Detection: Output sensitivity drift, offset drift or loss of function

Mitigation: The IC mold body needs to lie flat on the plastic housing. If the IC is upside-down, a nest shall be designed for the capacitor mold body (which is thicker than the Hall mold body)



Annex I: List of Abbreviations

AOI: Automatic Optical Inspection
BGA: Ball Grid Array
BTC: Bottom Terminated Components
CTE: Coefficient of Thermal Expansion
DFN: Dual Flat No-Leads
DMP: Dual Mold Package
FOD: Foreign Object Debris
HF: Halogen Free
IC: Integrated Circuit
NC: No clean
NPTH: Non-plated Through Hole
PCB: Printed Circuit Board
PCBA: Printed Circuit Board Assembly
QFN: Quad Flat No-Leads
QFP: Quad Flat Package
SIP: Single Inline Package
SMD: Surface Mount Devices
SMP: Single Mold Package
SMT: Surface Mount Technology
SOIC: Small Outline Integrated Circuit
SOT: Small Outline Transistor
SSOP: Shrink-Small Outline Package
TC: Thermal Cycles
TSSOP: Thin Shrink-Small Outline Package
UTDFN: Ultra Thin Dual Flat No-Leads
UV: Ultra Violet

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Annex II: List of Standards

J-STD-033: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

Annex III: List of related Application Notes

For the latest revision of this document and related Application Notes, visit www.melexis.com/ic-handling-and-assembly

Guidelines for storage and handling of plastic encapsulated ICs

Guidelines for Surface Mount Technology (SMT) soldering