Contents

1 Scope

This document describes the programming and End of Line calibration of the MLX90382 via the SPI slave interface of the sensor. In this document one will find the order of commands to successfully read and write parameters, store the content in the NVRAM, update the CRC of the NVRAM etc. This document also gives an overview of the NVRAM parameters grouped per function and more information on their application use case.

2 Related Melexis Products

MLX90382

3 Related Documents and Tools

MLX90382 Datasheet
MLX90382 API example code
MLX90382 Evaluation Kit
MLX90382 Safety Manual

4 SPI Protocol

General Description

The customer programming SPI slave interface allows read/write access to all ports/registers/memories, including the sensor position data. It operates at up to 10 MHz SPI clock full-duplex. The feature set is designed to support functional safety, continuous readout and multi-slave synchronization. The SPI supports all standard clock and phase modes to exchange data.

SPI Transaction for Register Read/Write Access

The exchange of data is possible with three different protocols. The structure of the protocols is shown in Figure 1. The transaction start with a 6-bit command pattern followed by the 10-bit address. In the following sub clauses, the function address size is noted as 10-bit, while the actual transferred address value is only 9-bit, omitting the LSB. This is due to the byte-wise notation of the MLX90382 address map (leading to 10-bit address range), while the access functions are word-wise (16-bit), such that the LSB-bit can be spared.

For Register Read (RR) and Register Write (RW), the 6-bit command pattern shall match exactly. In case of mismatch, the device always responds as in Frame Read (FR) mode.

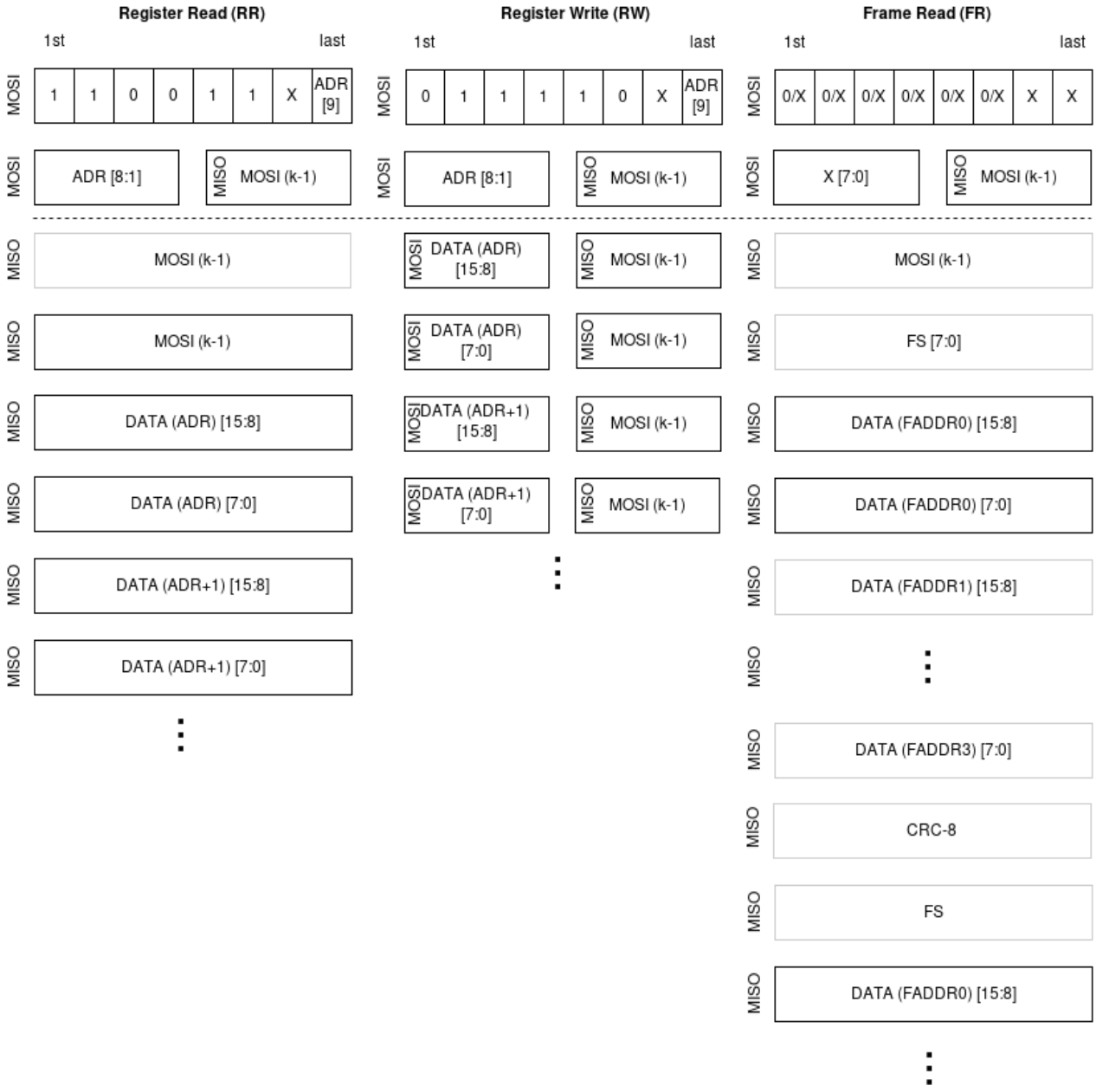

Figure 1: SPI Protocols for Read/Write and Frame Read.

4.1 Register Read (RR)

The register read operation starts by sending the command byte following the 9-bit aligned address [9:1]. The optional third byte allows adjusting the word alignment of the data transfer, **SPI_DMY**. The next byte acts as a dummy byte. Multiple words can be read in sequence, starting from the provided address.

	byte: k=0	1	2	3	4
MOSI	{7'b1100110, addr[9]}	addr[8:1]	x	x	x
MISO	Hi-Z	{7'b1100110, addr[9]}	MOSI(k-1)	rdata[15:8]	rdata[7:0]

Figure 2: SPI Protocols for read operation.

4.2 Register Write (RW)

The register write operation starts by sending the command byte following the 9-bit aligned address [9:1]. It allows access to all device registers. Multiple words can be written in sequence, starting from the provided address.

	byte: k=0	1	2	3
MOSI	{7'b0111100, addr[9]}	addr[8:1]	wdata [15:8]	wdata [7:0]
MISO	Hi-Z	{7'b0111100, addr[9]}	MOSI(k-1)	MOSI(k-1)

Figure 3: SPI Protocols for write operation.

4.3 Frame Read (FR)

It transmits the content of up to four register addresses, protected by an optional Frame Start (FS) byte and terminated by an optional CRC-8 byte. The register addresses for the read out can be configured by the user. The second address byte of the frame is ignored in the case of FR mode but still transmitted to prevent bus congestions in half-duplex mode and allow command fail checks on the ECU. The optional third byte allows adjusting the word alignment of the data transfer. A rolling counter defines the data of the optional FS byte. It will enable the detection of desynchronizations by the ECU (e.g. caused by lost SCLK edges). The optional CRC-8 byte protects the DATA fields.

4.3.1 SPI application mode, single slave

The SPI Frame read mode of the single slave starts by asserting CS=0 followed by the command 0x00 and the ignored address X. Note, any command value which is not SPI Register Read, SPI Register Write or SPI Super Frame Read is interpreted as SPI Frame Read.

	byte: k=0	1
MOSI	8'b00000000	x
MISO	Hi-Z	MOSI(k-1)

Figure 4: SPI application mode protocol, single slave SPI frame read start

The single Frame Read continues with reading N words from DSP addresses as configured in NV_SPI_FADDR0 ... NV_SPI_FADDR3 with SPI_FRFSEN and SPI_FRCRCEN. The SPI Frame Read mode is stopped by asserting CS=1.

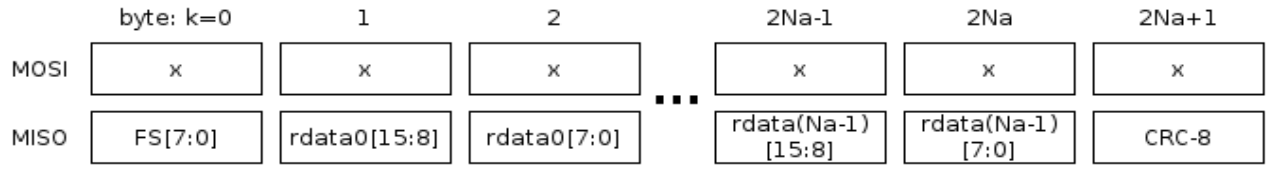

Figure 5: SPI application mode protocol, single slave SPI frame read

4.3.2 SPI application mode, multiple slaves

The SPI Super Frame read mode of the Multiple slave starts by asserting CS=0 followed by the command 0xC8 and the ignored address X.
The Super Frame Read continues with transmitting N words from the selected DSP addresses as configured in NV_SPI_FADDR0 ... NV_SPI_FADDR3 with SPI_FRFSEN and SPI_FRCRCEN of both slaves. The SPI Frame Read mode is stopped by asserting CS=1.

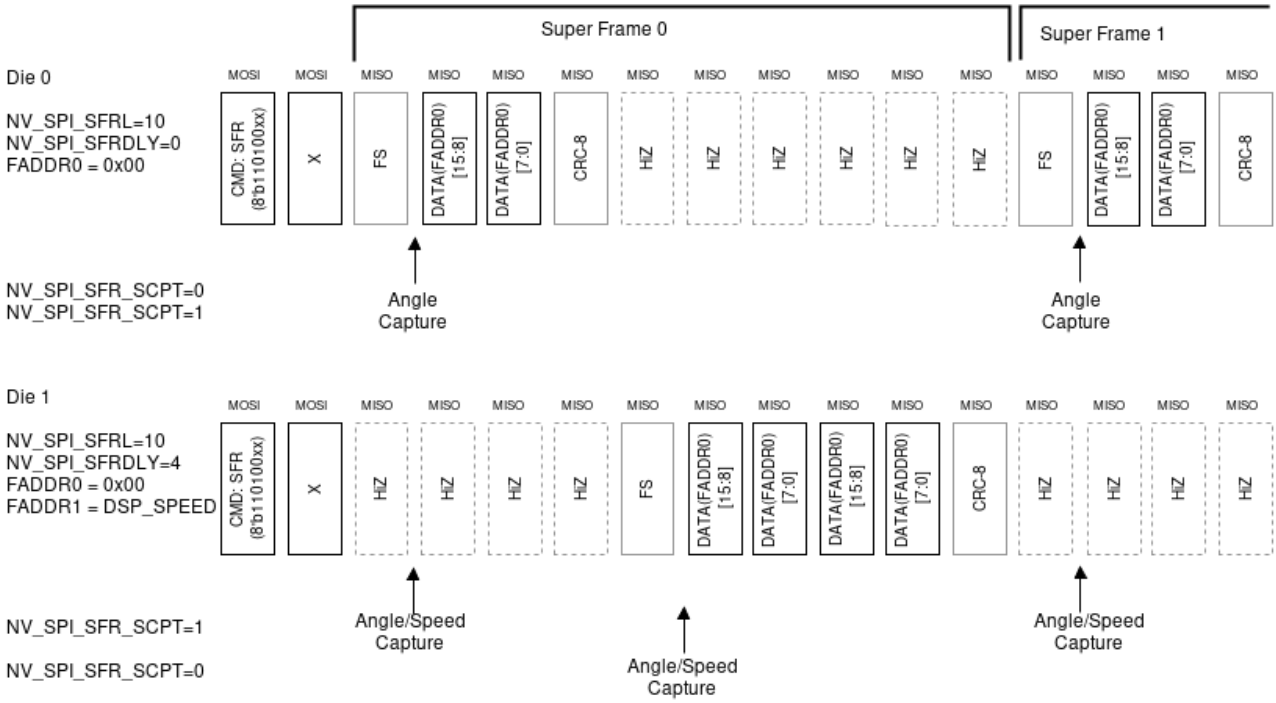

Figure 6: SPI application mode protocol, multiple slave

5 Control registers and macro commands

To read and write the NVRAM and registers of the MLX90382, a number of procedures, macro commands, have to be followed to gain access to the memory and to initiate the write procedure to the memory, specially the NVRAM.
Examples are the NVRAM store and lock command. For these commands one need to send a specific set of keys to execute the command.

To explain these procedures with examples, we use a set of commands to explain the working procedure to successfully execute a read, write, store, lock and frame read command. The command names are copied from the EVB programming tool instruction set that is available for the MLX90382. The procedure itself can be used in any µC with an SPI interface.

Command set:

:90382_SPI:Read:ADDRess	// Read N words from start address from mlx90382 memory: Number of words N <0...0xff>, Start address <0…0x2ff>
:90382_SPI:WRite:ADDRess	// Write N words from start to address from mlx90382 memory: Number of words N < 0...0xff>, Start address <0...0x2ff>, data <0...0xffff>
:90382_SPI:FRame:Start	// Frame mode Start mode for mlx90382
:90382_SPI:FRame:Read	// Single frame read of Na words from addresses as configured in mlx90382: Frame number of words of data <1...4>, Expected FS byte (0...0xFF)
:90382_SPI:FRame:End	// Stop SPI Frame Read
:90382_SPI:LLCHip:SElect	// Low level Chip Select
:90382_SPI:LLExchByte:Data <0...0xff>	// Low level read/write from mlx90382 memory. Single byte to write
:90382_SPI:LLCHip:DESelect	// Low level Chip De Select
:90382_SPI:NVm:STore part.	// NVRAM store procedure, transferring NVRAM SRAM content into NVM
:90382_SPI:NVm:LOck	// NVRAM lock procedure, protecting CUS section from modifications. NVM store procedure is included
:90382_SPI:GET:FW:VERSION	// Returns the current version of the firmware for mlx90382
:90382_SPI:SW:RESET	// Initializes a software reset for mlx90382
:SPIDB:CFG	// SPI Daughterboard config, CPOL, CPHA, CLK Pre-scaler (SCLK)
:SPIDB:CFG?	// Get SPI Daughterboard config, CPOL, CPHA, CLK Pre-scaler (SCLK)

5.1 Set Application Mode Inactive

Table 1: TEST Map – Application mode.

Field	Address	Bit	R/W	Description
-	36 0x0024	[15:3]	NU	Not used
DE_NVM_CRC		2	RW	Disable NVRAM CRC calculation
IN_APPLICATION		[1:0]	R/W	2: Application mode inactive, else: application mode active

Definition

The **IN_APPLICATION** parameter activates the DSP calculations of the sensor, application mode active. For the read and write access to the NVRAM the application mode needs to be set inactive during the SPI communication.

IMPORTANT. To ensure correct programming of the NVRAM or registers, it is important to verify if the parameter **IN_APPLICATION** is set to the correct value.

5.2 NVRAM Write Access

Table 2: DSP and EH Map – NVRAM Enter Programming Access

Field	Address	Bit	R/W	Description
-	16 0x0010	[15:4]	NU	Not used
NVOP_KEY		[3:0]	RW	8 bits KEY to unlock non-volatile operation. The key is 0x6B to be entered 4 bits per 4 bits (least nibble first)

Definition

The MLX90382 sensor has an 8 bits KEY to unlock non-volatile operation. This key needs to be set to gain write access to the NVRAM memory of the sensor. The key does not apply to read operations of Shadow Register operations.

5.3 Disable monitoring register and NVRAM

Table 3: DSP and EH Map – Monitoring of SR and NVRAM.

Field	Address	Bit	R/W	Description
-	36 0x0024	[15:3]	NU	Not used
DE_NVM_CRC		2	RW	Disable NVRAM CRC calculation
TEST_IN_APPLICATION		[1:0]	R/W	2: Application mode inactive, else: application mode active
EH_WD_EN	190 0x00BE	15	RW	If 1, warm reset is issued after 15ms in Hi-Z safe state
-		[14:10]	NU	Not used
Reserved		9	RW	Reserved, don't change.
DE_DSP_RMM		[9:7]	RW	Disable Residual mismatch correction: bit[1] - disable adaptive orthogonality correction bit[0] - disable adaptive sensitivity correction
DE_SCXY		6	RW	Disable SCXY errors
DE_INTP		5	RW	Disable INTP errors
DE_DIE		4	RW	Disable Crack detection error
DE_SR		[3:1]	RW	Disable Shadow Register Monitor. If 3, register monitor is disabled.
DE_AROC		0	RW	Disable AROC error

Definition

The MLX90382 sensor has a list of monitors that verify the functionality of the sensor. For functional safety the **DE_NVM_CRC**, **DE_SCXY**, **DE_INTP**, **DE_DIE, DE_SR** and **DE_AROC** monitors need to be ENABLED in the application. These parameters are only for debugging and programming the sensor. For more details, please refer to the functional safety manual of the MLX90382.

DE_NVM_CRC and **DE_SR** are used to monitor the memory of the sensor. During write access to the memory these monitors need to be switched off. Note that if one writes parameters in the SR, Shadow Register, **DE_SR** needs to remain disabled. If not, the changes in the SR register will be overwritten with the NVRAM content by the sensor.

If **EH_WD_EN** is set to 1, a warm reset is issued after 15ms in Hi-Z safe state. This command can be issued when the NVRAM is written. This command cannot be used when the SR is written, as the SR would be overwritten by the NVRAM values.

IMPORTANT. To ensure a correct programming of the NVRAM or registers, it is important to verify if the parameters **DE_NVM_CRC** and **DE_SR** are set to the correct value.

5.4 Update CRC NVRAM

Table 4: DSP and EH Map – CRC registers for NVRAM CRC update.

Field	Address	Bit	R/W	Description
CRC	38 0x0026	[15:0]	R	NVRAM checksum result
-	40 0x0028	[15:3]	NU	Not used
Reserved		2	RW	Reserved, do not change
CRC_CALC_DONE		1	R	If 1, NVRAM checksum computation finished, CRC updated
CRC_CALC_STRT		0	W	1: Start NVRAM checksum computation
CUS_CRC	606 0x025E	[15:0]	R/W	CUS area checksum (CRC16 CCITT)
-	16 0x0010	[15:4]	NU	Not used
NVOP_KEY		[3:0]	RW	8 bits KEY to unlock non-volatile operation. The key is 0x6B to be entered 4 bits per 4 bits (least nibble first)

5.4.1 SPI_NvmUpdateCRC ()

SPI_NvmUpdatesCRC, this procedure requests the sensor to recalculate the CRC of the NVRAM customer area. The new calculated CRC needs to be stored in the customer CRC address of the sensor.

```
:90382_SPI:Write:ADDRess 1, CRC_CALC_STRT_ADDRESS, 0x0001     //4. Initiate customer checksum calculation

wait (10 µs)                                                  //4a. Wait 10 µs for the CRC calculation

CRC_DONE = :90382_SPI:Read:ADDRess 1,                         //5. Check if the new CRC is calculated
CRC_CALC_DONE_ADDRESS

If CRC_DONE == TRUE                                           //6. Get the new CRC
   CRC = :90382_SPI:Read:ADDRess 1, CRC_ADDRESS

   :90382_SPI:Write:ADDRess 1, CUS_CRC_ADDRESS, CRC           //7. Store the new CRC in CUST_CRC area
   CUS_CRC = :90382_SPI:Read:ADDRess 1, CUS_CRC_ADDRESS

   If CUS_CRC != CRC                                          //7a. Verify if the CUS_CRC is written correctly
      :90382_SPI:Write:ADDRess 1, CUS_CRC_ADDRESS, CRC
```

5.5 Store NVRAM

Table 5: NVRAM Map - Registers to store content SR in NVRAM

Field	Address	Bit	R/W	Description
-	16 0x0010	[15:4]	NU	Not used
NVOP_KEY		[3:0]	RW	8 bits KEY to unlock non-volatile operation. The key is 0x6B to be entered 4 bits per 4 bits (least nibble first)
-	18 0x0012	[15:10]	NU	Not used
RECALL_REQ		9	RWE	Recall full array request. Automatically cleared at the end of the request. Not writable when a store or are call is in progress
STORE_REQ		8	RWE	Store low block request. Automatically cleared at the end of the request. Not writable when a store or are call is in progress
-		[7:2]	NU	Not used
DATA_CORRUPTED		1	RW1C	The data read is corrupted. It is due to a double error or a single bit error in the address.
SINGLE_ERROR_DETECTED		0	RW1C	A single bit error has been detected. The error can be in address, data or syndrome bit

5.5.1 SPI_NvmStore ()

NVRAM store procedure, transferring NVRAM SRAM content into NVM part.

```
:90382_SPI:Write:ADDRess 1, NVOP_KEY_ADDRESS, 0x000B          //8. Write key LSB nibble first

NVOP_KEY = :90382_SPI:Read:ADDRess 1, NVOP_KEY_ADDRESS        //8a. Verify key LSB content: if the
If NVOP_KEY != 0x000B                                          content does not match the
   :90382_SPI:Write:ADDRess 1, NVOP_KEY_ADDRESS, 0x000B        programmed content, repeat the
                                                               procedure

:90382_SPI:Write:ADDRess 1, NVOP_KEY_ADDRESS, 0x0006          //9. Write key MSB nibble first

NVOP_KEY = :90382_SPI:Read:ADDRess 1, NVOP_KEY_ADDRESS        //9a. Verify key MSB content: if the
If NVOP_KEY != 0x0006                                          content does not match the
   :90382_SPI:Write:ADDRess 1, NVOP_KEY_ADDRESS, 0x0006        programmed content, repeat the
                                                               procedure

:90382_SPI:Write:ADDRess 1, STORE_REQ_ADDRESS, 0x0100         //10. Initiate store request

wait (min. 15ms)                                              //11. Wait minimum 15ms
```

5.6 Lock NVRAM

Table 6: MCTRL Map – Register to start NVRAM locking.

Field	Address	Bit	R/W	Description
-	42 0x002A	[15:4]	NU	Not used
LOCK_KEY		[3:0]	WO1	Writing this register with sequence 0x7, 0x9, 0x4, 0xF will activate a procedure to write LOCK_EE[3:0] =0xA in NVRAM. Therefore, NVRAM will be locked for write access by the customer.

5.6.1 SPI_NvmLock ()

NVRAM lock procedure, protecting the customer section from modifications. The NVM store procedure is included.

```
:90382_SPI:Write:ADDRess 1, LOCK_KEY_ADDRESS, 0x0007          // Write LOCK KEY nibble 0

LOCK_KEY = :90382_SPI:Read:ADDRess 1, LOCK_KEY_ADDRESS        //Verify content: if the content does
If LOCK_KEY != 0x0007                                          not match the programmed content,
   :90382_SPI:Write:ADDRess 1, LOCK_KEY_ADDRESS, 0x0007        repeat the procedure

:90382_SPI:Write:ADDRess 1, LOCK_KEY_ADDRESS, 0x0009          // Write LOCK KEY nibble 1

LOCK_KEY = :90382_SPI:Read:ADDRess 1, LOCK_KEY_ADDRESS        // Verify content: if the content does
If LOCK_KEY != 0x0009                                          not match the programmed content,
   :90382_SPI:Write:ADDRess 1, LOCK_KEY_ADDRESS, 0x0009        repeat the procedure

:90382_SPI:Write:ADDRess 1, LOCK_KEY_ADDRESS, 0x0004          // Write LOCK KEY nibble 2

LOCK_KEY = :90382_SPI:Read:ADDRess 1, LOCK_KEY_ADDRESS        // Verify content: if the content does
If LOCK_KEY != 0x0004                                          not match the programmed content,
   :90382_SPI:Write:ADDRess 1, LOCK_KEY_ADDRESS, 0x0004        repeat the procedure

:90382_SPI:Write:ADDRess 1, LOCK_KEY_ADDRESS, 0x000F          // Write LOCK KEY nibble 3

LOCK_KEY = :90382_SPI:Read:ADDRess 1, LOCK_KEY_ADDRESS        // Verify content: if the content does
If LOCK_KEY != 0x000F                                          not match the programmed content,
   :90382_SPI:Write:ADDRess 1, LOCK_KEY_ADDRESS, 0x000F        repeat the procedure

Wait (min. 15ms)                                               // Wait minimum 15ms
```

5.7 SPI_Read()

For a reading of the NVRAM, the sensor's application mode needs to be set inactive. After that a single address or multiple addresses can be read from the MXL90382 memory.

```
:90382_SPI:Write:ADDRess 1, IN_APPLICATION_ADDRESS, 0x0002    // Set application mode inactive

Data = :90382_SPI:Read:ADDRess N, Start Address               // Read a Number of sequential
                                                               addresses

:90382_SPI:Write:ADDRess 1, IN_APPLICATION_ADDRESS, 0x0000    // If needed, set application mode
                                                               active
```

5.8 SPI_Write()

For writing the NVRAM, the sensors application mode, NVRAM CRC check and register monitoring needs to be set inactive. After that a single address or multiple addresses can be programmed. Followed by a CRC update and the store command of the MLX90382.

Table 7: Programming sequence for SPI_Write

Step	Register Bit	Address	Bit Position	Access	Register Value	Comment
1	DE_NVM_SR	0x0BE	[3:1]	WR	3	Stop updating shadow registers from NVRAM
1.a				RD	3	Verify DE_NVM_SR content: if the content does not match the programmed content, repeat the procedure
2	DE_NVM_CRC IN_APPLICATION	0x024	2 [1:0]	WR	1 2	Stop automatic NVRAM CRC calculation Stop application
2.a				RD	6	Verify IN_APPLICATION and DE_NVM_CRC content: if the content does not match the programmed content, repeat the procedure
3	<NVRAM bit(s)>			WR	<TBD>	Write new NVRAM content within user register map range, refer to MLX90382 datasheet
3.a				RD	<TBD>	Verify NVRAM bit(s) content: if the content does not match the programmed content, repeat the procedure
4	CRC_CALC_STRT	0x028	0	WR	1	Initiate customer checksum calculation
5	CRC_CALC_DONE	0x028	1	RD	1	If 1, NVRAM checksum computation is finished and the CRC is updated.
6	CRC	0x026	[15:0]	RD	CRC	Read customer checksum
7	CUS_CRC	0x25E	[15:0]	WR	CRC	Write customer checksum in NVRAM
7.a				RD	CRC	Verify CUS_CRC content: if the content does not match the programmed content, repeat the procedure
8	NVOP_KEY	0x010	[3:0]	WR	0x0B	Write key LSB nibble first (incl. in SW API SPI_NvmStore())
8.a				RD	0x0B	Verify key LSB content: if the content does not match the programmed content, repeat the procedure
9	NVOP_KEY	0x010	[3:0]	WR	0x06	Write key MSB nibble second (incl. in SW API SPI_NvmStore())
9.a				RD	0x06	Verify key MSB content: if the content does not match the programmed content, repeat the procedure
10	STORE_REQ	0x012	8	WR	1	Initiate store request (incl. in SW API SPI_NvmStore())
11						Wait min. 15ms (incl. in SW API SPI_NvmStore())
12						Perform a power cycle to check the new NVRAM content

:90382_SPI:Write:ADDRess 1, DE_SR_ADDRESS, 0x0003	//1. Set DE_SR to disable shadow register monitoring
DE_SR = :90382_SPI:Read:ADDRess 1, DE_SR_ADDRESS If DE_SR != 0x0003 :90382_SPI:Write:ADDRess 1, DE_SR_ADDRESS, 0x0003	//1a. Verify content: if the content does not match the programmed content, repeat the procedure
:90382_SPI:Write:ADDRess 1, ADDRESS 0x024, 0x0006	//2. Set application mode inactive Set DE_NVM_CRC to disable NVRAM CRC calculation
VALUE = :90382_SPI:Read:ADDRess 1, ADDRESS 0x024 If VALUE != 0x0006 :90382_SPI:Write:ADDRess 1, ADDRESS 0x024, 0x0006	//2a. Verify content: if the content does not match the programmed content, repeat the procedure
:90382_SPI:WRite:ADDRess N, Address, Data1, Data2, …	//3. Write a Number of sequential address
Data[N] = :90382_SPI:Read:ADDRess N, Start Address If Data[N] != Data1, Data2, … :90382_SPI:WRite:ADDRess N, Address, Data1, Data2, …	//3a. Read the sequential addresses: if the content does not match the programmed content, repeat the procedure
:90382_SPI:Write:ADDRess 1, CRC_CALC_STRT_ADDRESS, 0x0001	//4. Initiate customer checksum calculation
wait (10 µs)	//4a. Wait 10 µs for the CRC calculation
CRC_DONE = :90382_SPI:Read:ADDRess 1, CRC_CALC_DONE_ADDRESS	//5. Check if the new CRC is calculated
If CRC_DONE == TRUE CRC = :90382_SPI:Read:ADDRess 1, CRC_ADDRESS	//6. Get the new CRC
:90382_SPI:Write:ADDRess 1, CUS_CRC_ADDRESS, CRC CUS_CRC = :90382_SPI:Read:ADDRess 1, CUS_CRC_ADDRESS	//7. Store the new CRC in CUST_CRC area
If CUS_CRC != CRC :90382_SPI:Write:ADDRess 1, CUS_CRC_ADDRESS, CRC	//7a. Verify if the CUS_CRC is written correctly
:90382_SPI:NVm:Store	//8 - 11. Store NVRAM command

6 Device configuration with NVRAM

6.1 Application modes

Table 8: NVRAM map - Application modes

Field	Address	Bit	R/W	Description
SENSING_MODE	512 0x0200	[2:0]	R/W	Magnetic sensing mode: 0: X-Y 1: X-Z, 2: Y-Z
GPIO_IF		[4:3]	R/W	GPIO protocol: 0: PWM/Differential ABI or differential UVW, 1: SSI; 2: SPI bus mode
ABI_IF		5	R/W	ABI / UVW protocol: 0: UVW; 1: ABI
ABI_DIFF		6	R/W	ABI/UVW differential mode: 0: single ended mode, 1: differential mode
GPIO_CFG		[11:7]	R/W	GPIO output driver configuration [9:7] driver strength, see definitions. [11:10] driver-mode: 0: off, 1: open-drain p-MOS, 2: open-drain n-MOS, 3: push-pull.
-		[15:12]	NU	Not used
ABI_CFG	514 0x0202	[4:0]	R/W	ABI output driver configuration [2:0] driver strength, see definitions. [4:3] driver-mode: 0: off, 1: open-drain p-MOS, 2: open-drain n-MOS, 3: push-pull.
EH_MIN_SS_PERIOD		[7:5]	R/W	Minimum safe state period. Please refer to the MLX90382 safety manual for details.
-		[15:8]	NU	Not used

Definition

The address that configures the application mode sets 2 properties, the input and the output properties of the application.
The input is defined by the NVRAM parameter **SENSING_MODE**. For the order code 600 the hall plates are set in dBz mode. In this configuration the value of the **SENSING_MODE** is not used by the sensor.

Table 9: Sensing modes

Option Code	dBz	SENSING_MODE	Sensing modes	Field cos (I)	Field sin (Q)
000/100	0	0	ROTARY_XY	Bx	By
000/100	0	1	ROTARY_XZy	Bx	Bzy
000/100	0	2	ROTARY_YZx	By	Bzx
60x	1	x	ROTARY_XY @ dBz circle	dBzx	dBzy

The output is defined by the parameters **GPIO_IF** and **ABI_IF**. The two parameters allow one to configure 2 different output protocols to report the sensor data simultaneously.

The QFN-24 package provides a differential ABI and differential UVW interface output, meaning the ABI/UVW signals are logical inverted, with signal levels ranging between VSS and VDD. By configuring **ABI_DIFF** to 1, the inverted signals A/U_N, B/V_N and I/W_N are provided at the AU_N, SCLK and MOSI pins, respectively.

This also means that the B and I signals are connected to the SCLK and MOSI pin of the companion µC. Therefor the SPI port of the µC needs to be disconnected from the sensor or set in high-Z mode when the sensor is in application mode, CS = 1, this to avoid a short between the ABI drivers of the sensor and the SPI port of the µC. With CS = 0 the SPI port can be enabled again to communicate with the sensor.

GPIO_CFG and **ABI_CFG** are 5-bit parameters to configure the output driver mode. 2 bits are used to set the driver mode; 0: off, 1: open-drain p-MOS, 2: open-drain n-MOS, 3: push-pull. 3 bits are used to trim the driver strength.
The purpose of the trimming is to limit the driver strength to avoid an overload on the output in case of a short circuit.
The factory trimmed driver strength is for 5V applications. For 3V3 applications, this factory trimmed setting results in a lower driver strength. Therefore, the driver strength might be adapted for 3V3 applications. In 3V3 applications the maximum allowed driver strength is 7. For 5V applications, the factory trimmed value is the maximum allowed driver strength. A higher value can lead to damage in 5V mode in case the driver pin is shorted. Therefore, if one wants to run tests/experiments on both 3V3 and 5V, it is advised to log the 5V driver strength.

Table 10: Driver strength GPIO and ABI/UVW pins

GPIO_CFG[9:7] - ABI_CFG[2:0]	Description
0	Off (Hi-Z)
1	Minimum driver strength.
2	
3	
4	Used test condition datasheet for VDD 5V
5	
6	
7	Maximum driver strength. Used test condition datasheet for VDD 3V3

6.2 UVW configuration

Table 11: NVRAM map - UVW configuration parameters

Field	Address	Bit	R/W	Description
ABI_LOG2N	516 0x0204	[3:0]	R/W	ABI log2(N), where N is the number of periods A/B per 360 deg.
UVW_PP		[8:4]	R/W	UVW pole pairs 1-32
ABIUVW_DIR		9	R/W	ABI / UVW rotation direction CW-CCW
ABIUVW_HYS		[13:10]	R/W	ABI / UVW hysteresis: ±floor(2^(ABIUVW_HYS-1))
ABI_I_LEN		14	R/W	ABI I-pulse length selection
ABI_PORT		15	R/W	QFN-24 ABI/UVW pin group selection: 0: select pin group AU_N, SCLK and MOSI 1: select pin group AU, BV and IW

Definition

The MLX90382 UVW interface emulates the signals which are generated by the three discrete Hall switches used in BLDC motors. The number of pole pairs of the motor is programmable from 1 to 32 pairs with the **UVW_PP** parameter. The UVW signals are calculated based on the 16-bit estimated, delay compensated angular value. A dedicated hysteresis allows to avoid toggling transitions and is adjustable, **ABIUVW_HYS**, in a wide range to optimize noise versus accuracy. The direction of rotation can be reversed with **ABIUVW_DIR**. **ABI_PORT** sets the ABI/UVW pin group used for the output. This function is disabled on the TSSOP package.

If **ABI_PORT** = 0 the B and I signals are connected to the SCLK and MOSI pin of the companion µC. Therefor the SPI port of the µC needs to be disconnected from the sensor or set in high-Z mode when the sensor is in application mode CS = 1, this to avoid a short between the ABI drivers of the sensor and the SPI port of the µC. With CS = 0 the SPI port can be enabled again to communicate with the sensor.

6.3 ABI configuration

Table 12: NVRAM map - ABI configuration parameters

Field	Address	Bit	R/W	Description
ABI_LOG2N	516 0x0204	[3:0]	R/W	ABI number of counts per revolution with: 4 * 2^{ABI_LOG2N} per 360°
UVW_PP		[8:4]	R/W	UVW pole pairs
ABIUVW_DIR		9	R/W	ABI / UVW rotation direction CW-CCW
ABIUVW_HYS		[13:10]	R/W	ABI / UVW hysteresis: ±floor(2^(ABIUVW_HYS-1))
ABI_I_LEN		14	R/W	ABI I-pulse length selection, 0 = 1 count, 1 = 3 counts long.
ABI_PORT		15	R/W	QFN-24 ABI/UVW pin group selection: 0: select pin group AU_N, SCLK and MOSI 1: select pin group AU, BV and IW

Definition

The MLX90382 supports an incremental output with three signals. A and B are the quadrature signals, and I is the reference mark which indicates one revolution. The number of periods, **ABI_LOG2N**, is programmable up to 2^{12} pulses per rotation. A dedicated hysteresis, **ABIUVW_HYS**, allows to avoid toggling transitions and is adjustable in a wide range to optimize noise versus accuracy. The direction of rotation can be reversed with **ABIUVW_DIR**. With **ABI_I_LEN** = 0, the I pulse length is 1 count long. With **ABI_I_LEN** = 1, the I pulse length is 3 counts long. **ABI_PORT** sets the ABI/UVW pin group used for the output. This function is disabled on the TSSOP package.

If **ABI_PORT** = 0 the B and I signals are connected to the SCLK and MOSI pin of the companion µC. Therefor the SPI port of the µC needs to be disconnected from the sensor or set in high-Z mode when the sensor is in application mode → CS = 1, this to avoid a short between the ABI drivers of the sensor and the SPI port of the µC. With CS = 0 the SPI port can be enabled again to communicate with the sensor.

Note that the number of periods per rotation and the hysteresis has to be limited in function of the rotation speed of the application. The configuration for **ABI_LOG2N** and **ABIUVW_HYS** vs. speed and acceleration needs to ensure that:

$$\frac{V_{el}}{f_{AC}} * 2^{16} < 2^{14-ABI_{LOG2N}-ABIUVW_{HYS}-1}$$

Where:

$$f_{AC} = 20MHz$$

This formula limits the max rotational speed dependent on the ABI settings for the number off pulses and the supported hysteresis. The hysteresis value needs to be set higher than the expected peak noise. The recommended **ABIUVW_HYS** setting is 5 or higher.

The configuration of **ABI_LOG2N** and **ABIUVW_HYS**, as described in the datasheet, is constrained by the maximum angular speed v_{el} and also by the angular noise, which is influenced by the bandwidth of the internal tracking filter. The bandwidth is determined by the LFC settings, which must be considered when selecting the number of pulses N_{ABI_PULSE}. **ABI_LOG2N** must be limited according to the setting in **DSP_LFC_HI** and the operating performance conditions.

E.g. For 2^{12} periods per rotation, the rotational speed is limited to 4577RPM, for a hysteresis setting of 5 and a filter setting of 0. For a hysteresis setting of 6 and a filter setting of 3, the rotational speed is limited to 2288RPM.

6.4 PWM configuration

Table 13: NVRAM map – PWM configuration parameters

Field	Address	Bit	R/W	Description
PWM_INV	518 0x206	0	R/W	PWM waveform inversion
PWM_PCNT_ON		1	R/W	PWM period counter (PWM_PCNT), 0: period counter off, 1: PWM counter running despite GPIO_IF setting
Reserved		[7:2]	R/W	Reserved, don't change.
-		[15:8]	NU	Not used
PWM_PERIOD	558 0x22E	[15:0]	R/W	PWM period
PWM_DC_OFS	584 0x248	[8:0]	R/W	PWM Duty Cycle offset trimming. See DSP configuration.
-		[15:9]	NU	Not used

Definition

The MLX90382 performs pulse width modulation (PWM) with a time resolution of $1/f_{AC}$. The interface supports a free programmable period and duty cycle range. The total period T_{PWM} is configurable, **PWM_PERIOD**, and depends on the application clock frequency f_{AC}. The PWM duty cycle T_{PWM_ON} is proportional to the angular value after signal conditioning and interpolation, captured at the beginning of the PWM period. The PWM waveform can be inverted with **PWM_INV**. With the **PWM_PCNT_ON** setting, the PWM counter is turned on in case the PWM output is not selected with the GPIO_IF setting. This is used for synchronization between the Main Clock Frequency fRCO /ECU clock frequency synchronization on item level. **PWM_DC_OFS** compensates for a mismatch between rising and falling edge delays of the PWM signal caused by the trigger level of the PWM measurement. The signed field **PWM_DC_OFS** allows adjusting the T_{PWM_ON} time by ΔT_{PWM_ON} = **PWM_DC_OFS**/f_{AC}. **PWM_DC_OFS** allows adjustment within ±12.8us with 50ns resolution for f_{AC}=20MHz.

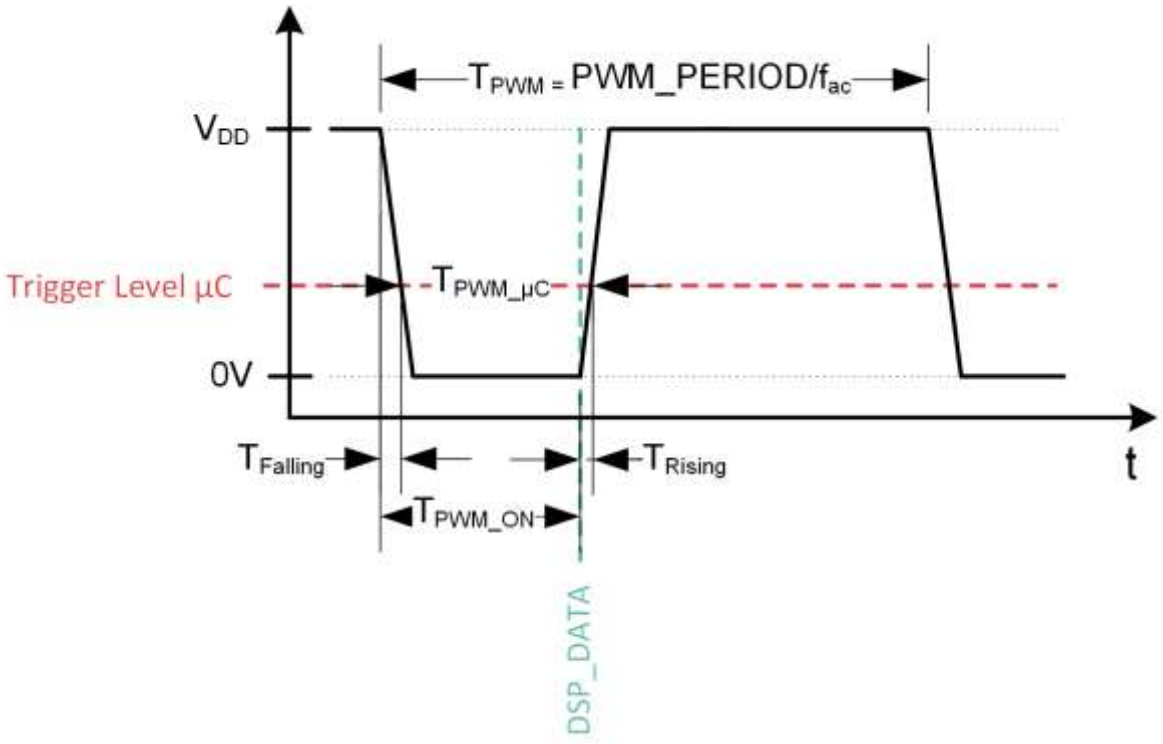

Figure 7: PWM_DC_OFS

6.5 SPI configuration

Table 14: NVRAM map – SPI configuration parameters

Field	Address	Bit	R/W	Description
SPI_FADDR0	560 0x0230	[7:0]	R/W	SPI FR Address 0
SPI_FADDR1		[15:8]	R/W	SPI FR Address 1
SPI_FADDR2	562 0x0232	[7:0]	R/W	SPI FR Address 2
SPI_FADDR3		[15:8]	R/W	SPI FR Address 3
SPI_FRFS	564 0x0234	[3:0]	R/W	SPI FR frame start pattern
SPI_FRFSEN		4	R/W	SPI FR frame start enabled
SPI_FRCRCEN		5	R/W	SPI FR CRC enable
SPI_FRINV		[9:6]	R/W	SPI FR data inversion
SPI_MODE		[11:10]	R/W	SPI mode selection {CPOL, CPHA}
SPI_DMY		[13:12]	R/W	SPI output optional word alignment
-		[15:14]	NU	Not used
SPI_SFRL	566 0x0236	[7:0]	R/W	SPI super frame length
SPI_SFRDLY		[15:8]	R/W	SPI FR delay within super frame
SPI_CPTLT	568 0x0238	[2:0]	R/W	SPI capture lead time synchronous (SPI_CPTLT + 1) * TSCLK before the "DATA (FADDR0) [15:8]"-byte
SPI_SFR_SCPT		3	R/W	Synchronize the angle/speed capture time point on all slaves to the position of the DATA(FADDR0) [15:8] byte with SPI_SFRDLY = 0
SPI_DBNC_CS		[7:4]	R/W	SPI CS debounce filter τCS = SPI_DBNC_CS*2/f_{RCO}
SPI_DBNC		[11:8]	R/W	SPI SCLK/MOSI debounce filter τSCLK/MOSI = SPI_DBNC/f_{RCO}
-		[15:12]	NU	Not used
PHY_RC_EN	572 0x23C	[2:0]	R/W	EMC RC filter enable: Bit[0]: pin CS Bit[1]: pin IW (QFN-24)/pin MOSI (TSSOP-16/ TSSOP-16_EP) Bit[2]: pin BV (QFN-24)/pin SCLK (TSSOP-16/ TSSOP-16_EP)
PHY_CS_RPU_DIS		3	R/W	Pin CS pull-up disable
PHY_BV_RPU_DIS		4	R/W	BV Pad pull-up disable (SCLK)
Reserved		[6:5]	R/W	Reserved, don't change.
Not used		[15:7]	R	

Definitions

The SPI slave interface for customer programming allows read/write access to all registers and memories, including the sensor position data. It operates up to 10MHz SPI clock full-duplex and is designed to support functional safety, continuous readout and multi-slave synchronization. The SPI supports all standard clock and phase modes to exchange data. SPI clock polarity and phase are defined by the parameter **SPI_MODE** according to the table below.

Table 15: SPI MODE

SPI_MODE [1:0]	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

The SPI input pins are equipped with a debounce filter. The filter can be configured with the following parameters.

SPI_DBNC_CS set the debounce filter of the CS pins of the SPI hardware layer.

$$\tau_{CS} = \frac{SPI\_DBNC\_CS * 2}{f_{RCO}}$$

SPI_DBNC set the debounce filter of the input pins of the SPI hardware layer.

$$\tau_{SCLK/MOSI} = \frac{SPI\_DBNC * 2}{f_{RCO}}$$

The SPI allows for synchronous capturing and sequential transmission of angular data with multiple SPI slaves on a shared MISO bus, as described in the datasheet. This specific mode can only be used in combination with the SPI debounce register setting **SPI_DBNC** = 2 for all MLX90382ABA slave devices to avoid potential protocol violation. The debounce function introduces a delay between SPI master clock SCLK and the SPI slave MISO response, as described in the datasheet.

PHY_RC_EN enables the RC filter on the SPI pins.
PHY_CS_RPU_DIS disables the pull-up on the SPI CS pin. **PHY_BV_RPU_DIS** disables the pull-up on the SPI SCLK pin.
SPI_DMY Sets a SPI output optional word alignment, as illustrated in Figure 1: SPI Protocols for Read/Write and Frame Read.
SPI_CPTLT allows one to change angle capture points within the SPI FR and SFR. The capture point is defined in TSCLK clocks before the "DATA (FADDR0) MSB"-byte.

$$Angle\ Capture\ Point = (SPI\_CPTLT + 1) * (TSCLK\ CLOCK\ CYCLES)$$

To ensure compliance with bus timing requirements, it is necessary to adjust SPI_CPTLT accordingly:

$$SPI\_CPTLT \geq 5 \cdot \frac{f_{SCLK}}{f_{ac}} - 0.5$$

The following set of SPI parameters are used to configure the continuous readout, SPI Frame Read (FR) mode and SPI Super Frame Read (SFR). When the GPIO_IF = SPI_BUS_MODE the sensor allows continuous readout of DSP data while CS=0. Frame Read transmits the content of up to four register addresses, protected by an optional Frame Start (FS) byte SPI_FRFSEN and terminated by an optional CRC-8 byte, SPI_FRCRCEN. The register addresses for the read out can be configured by the user by **SPI_FADDR0**, **SPI_FADDR1**, **SPI_FADDR2** and **SPI_FADDR3**.

The FS byte defines the start data of the frame. It will enable the possibility to detect desynchronization by the ECU (e.g. caused by lost SCLK edges). **SPI_FRFS** sets the SPI FR frame start pattern FS [7:0] which is composed of the frame start pattern FS [7:4] = **SPI_FRFS** (default 4'b1010), followed by a 4-bit rolling counter FS [3:0] = RC [3:0]. The rolling counter is updated on every frame transmitted, also in case the sensor is determined to be in error condition and also when the frame content with the application layer data is not updated.

The optional CRC-8 byte protects the DATA fields. The SPI FR optional CRC-8-CCITT is calculated with a polynomial = 0x07, initial value = 0xFF and final XOR value = 0x00.

$$Polynomial = x\text{^}8 + x\text{^}2 + x\text{^}1 + 1$$

This sequence is continued until CS=1. DATA (FADDR1), DATA (FADDR2), DATA (FADDR3) are transmitted only, if the corresponding SPI_FADDRx is non-zero respectively. DATA (FADDR0) transmits the sensor angle unless SPI_FADDR0 is non-zero. DATA (FADDRx) is inverted, if bit x of the 4-bit **SPI_FRINV** parameter is set to 1 (mask), this allows alternative re-transmission checks, in case CRC-8 is not used.
DATA (FADDR1), DATA (FADDR2), DATA (FADDR3) are typically programmed to report data from Digital Signal

Processing data addresses. The SPI Frame Read and the SPI Super Frame Read can also report data from the NVRAM or EH_MST data addresses. For example, part of the USER_ID0…5 or the Diagnostic registers.

Note that to fit the 9-bit address in the 8-bit register the LSB is dropped. The address is shifted one bit, Address >> 1.
So, **SPI_FADDR0**, **SPI_FADDR1**, **SPI_FADDR2** and **SPI_FADDR3** = Address [8:1].

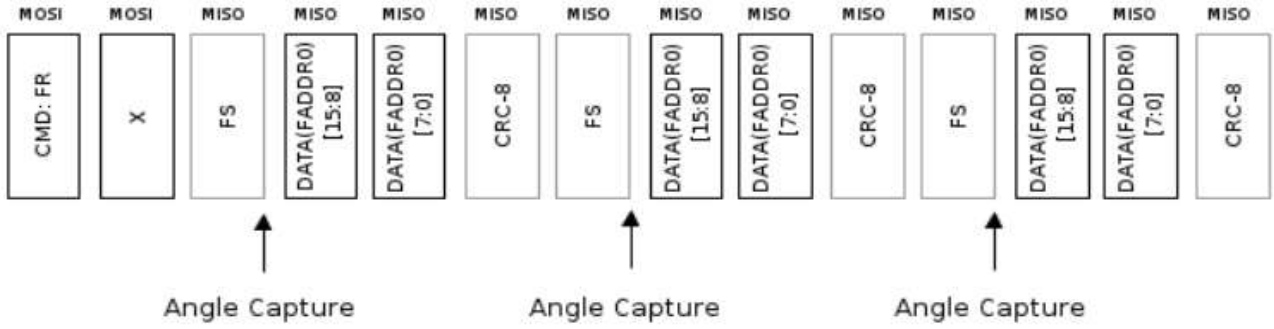

Figure 8: SPI Frame Read (FR) synchronous data sampling

The figure above illustrates the following sequence:

```
:90382_SPI:FRame:STart          // Frame mode Start mode for mlx90382, CS=0, CMD: FR, X

for i=0; i<3; i++
{
        :90382_SPI:FRame:Read 1, 0
                                // Single frame read of Na words from addresses as configured in mlx90382:
                                Frame number of words of data <1...4>, Expected FS byte (0...0xFF)
}

:90382_SPI:FRame:End            // Stop SPI Frame Read, CS = 1
```

The MLX90382 SPI interface supports an optional synchronous readout of multiple devices. The definition of the Frame Read (FR) Super Frame and the delayed transmission of the FR response frame allows a time-division-multiple-access scheme (TDMA) on MISO supporting up to 16 SPI slaves to capture/measure synchronized while transmitting the data sequentially on the shared MISO bus line. A typical use-case is the dual-die product configuration at the TSSOP16eP package.

With field **SPI_SFRL** (Customer default=0), the SPI super frame (SFR) shall be defined that allows synchronous capturing and sequential transmission of angular data with multiple SPI slaves on a shared MISO bus. The **SPI_SFRL** FR response frame length (excluding the 2 MOSI bytes) is defined as:

$$L_{Frame} = SPI\_FRFSEN + 2 \times \left(1 + (SPI\_FADDR1 \neq 0) + (SPI\_FADDR2 \neq 0) + (SPI\_FADDR3 \neq 0)\right) + SPI\_FRCRCEN$$

The SFR length for N SPI slaves then should be the sum of all frame lengths:

$$SPI\_SFRL = \sum_{n=1}^{N} L_{Frame}$$

A super frame length configured with a nonmatching **SPI_SFRL** disables the super frame.
With field **SPI_SFRDLY** (Customer default=0), the device shall delay the transmission of a single FR response frame (on MISO) within the SFR super frame by **SPI_SFRDLY** bytes. Before and after the single frame transmission within the FR Super Frame the SPI MISO shall be Hi-Z.

SPI_SFR_SCPT allows one to synchronize the angle/speed capture time point on all slaves to the position of the DATA(FADDR0) [15:8] byte with SPI_SFRDLY = 0, the first sensor.

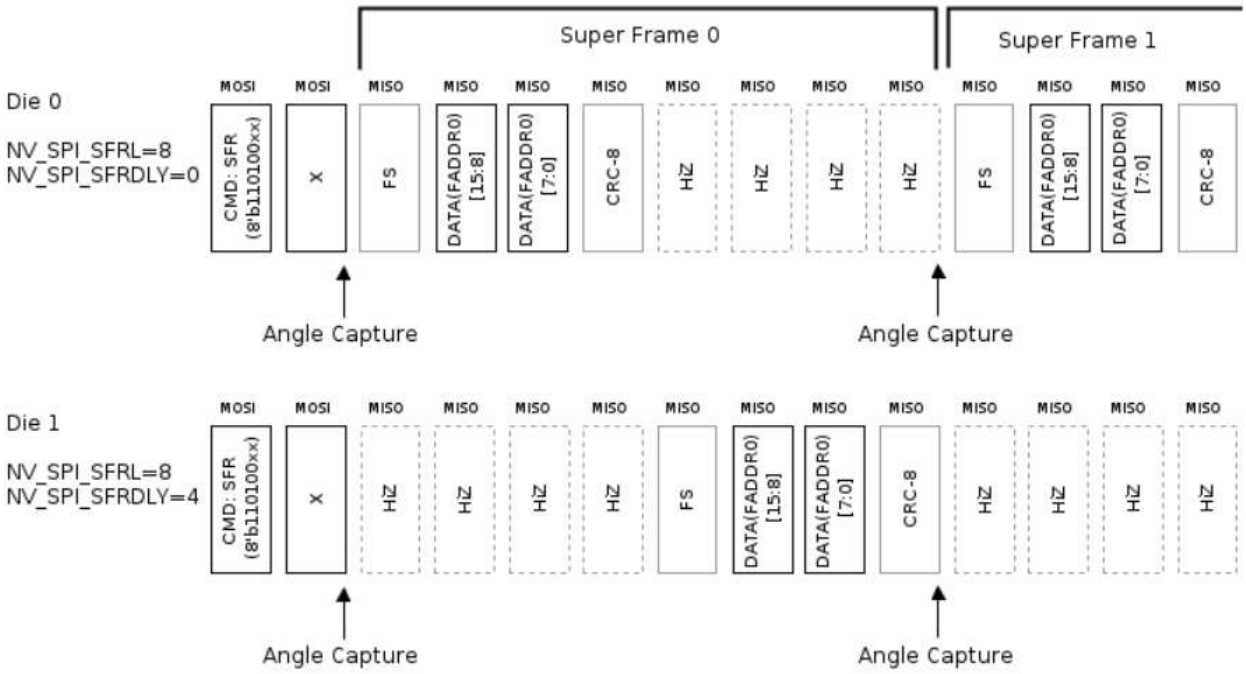

Figure 9: SPI protocol for synchronous readout of multiple slaves

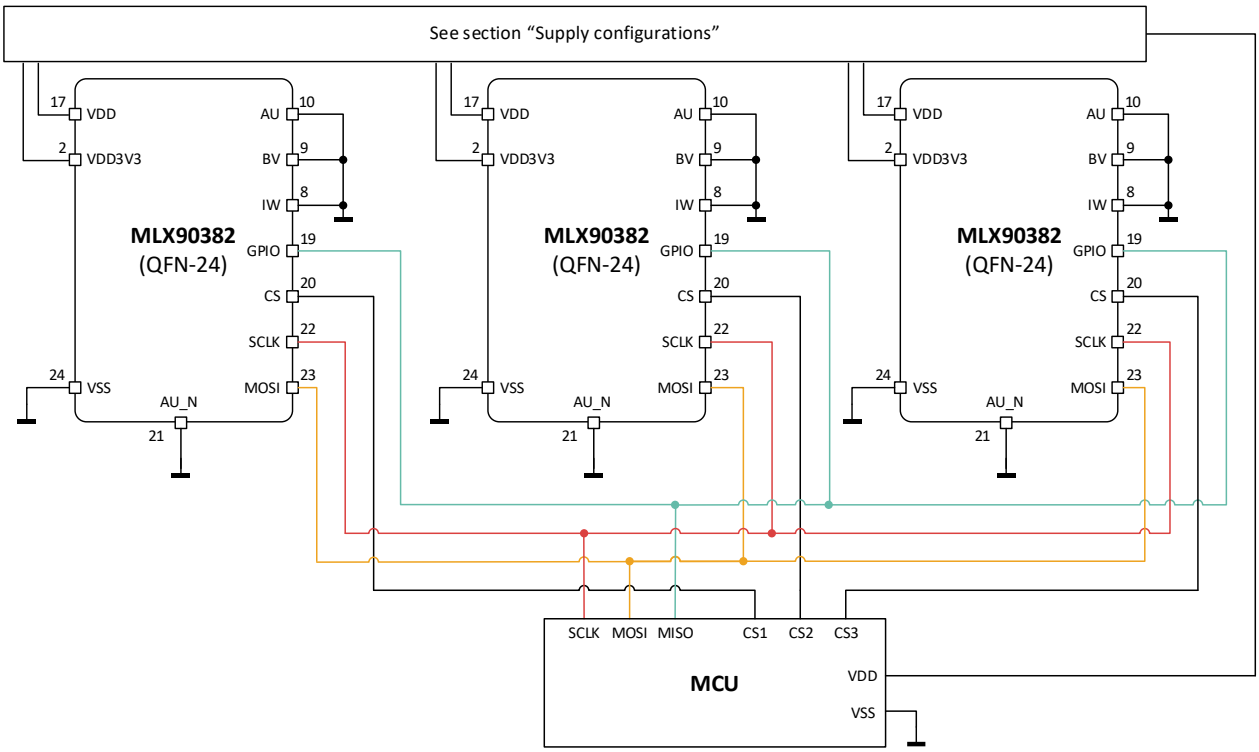

Figure 10: Example SPI connection diagram of multiple slaves

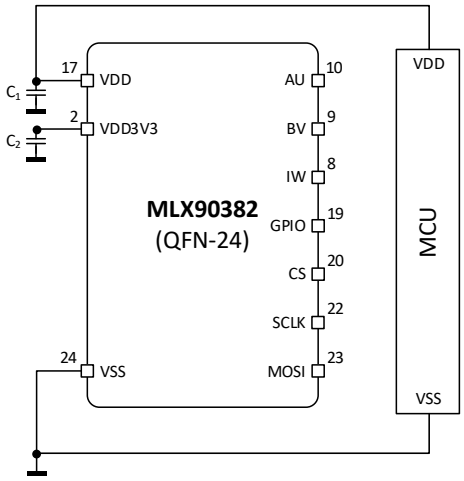

Figure 11: Example depicting 5 V supply mode

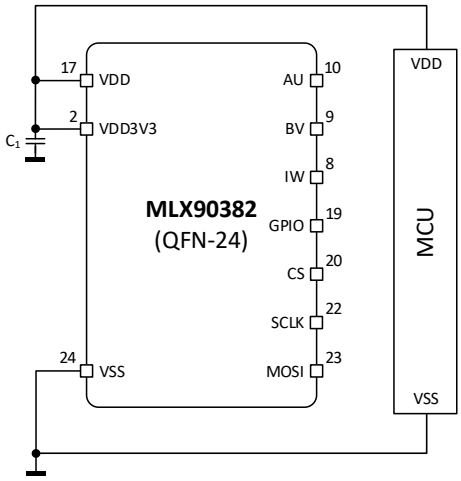

Figure 12: Example depicting 3.3 V supply mode

6.6 SSI configuration

Table 16: NVRAM map – SSI configuration parameters

Field	Address	Bit	R/W	Description
SSI_PARPOS	570 0x023A	[3:0]	R/W	SSI parity bit position: ≤ 8: parity of angle[15 : SSI_PARPOS+1] transmitted at bit position SSI_PARPOS > 8: no parity bit - SSI data: angle[15:0]
SSI_TM		[11:4]	R/W	SSI timeout, TM = (SSI_TM+1)*8/f_{AC}
SSI_CPT		12	R/W	In SSI normal mode (SSI_FR = 0), the DSP output shall be sampled at rate f_{AC} depending on SSI_CPT (CUS, default: 0) as follows: SSI_CPT = 0: falling edge on SCLK after start-up and falling edge after pause pulse (TP) SSI_CPT = 1: After TM counting from rising edge of pause pulse (TP)
-		[15:13]	NU	Not used

Definition

Via SSI default mode, the angular value is transmitted as a 16-bit word composed of a 15-bit 2s-complement value after signal conditioning and interpolation and an optional parity bit. The position of the parity bit can be defined within the 16-bit frame with **SSI_PARPOS**. That allows the ECU to optimize the frame rate. With **SSI_PARPOS** > 8, no parity bit is set and the SSI data is a 16-bit angle[15:0]. With **SSI_PARPOS** ≤ 8, a parity is added at bit position **SSI_PARPOS** to the SSI data. The angle data is limited to angle[15:SSI_PARPOS+1].

Table 17: MLX90382ABA SSI Frame composition with parity bit

Bit Position	15	SSI_PARPOS+1	SSI_PARPOS	SSI_PARPOS-1	0
Content	$\varphi_{sc}[15: SSI\_PARPOS+1]$		Parity-Bit	to be ignored	

It can be seen that the information inside φ_{sc} undergoes a bit shift: $\varphi_{sc} >> (SSI\_PARPOS+1)$, which can be expressed as the operation: $floor\left(\frac{\varphi_{sc}}{2^{SSI\_PARPOS+1}}\right)$. This affects all related information, such as the angular value and in case of signal conditioning the defined thresholds for SC_YE and SC_HL and the scaled output angle.

Signal conditioning need to be applied to scale the angular value into the desired range $\varphi_{sc}[15: SSI\_PARPOS+1]$. Following constraints must be fulfilled to avoid placing the parity bit into the scaled output data range of φ_{sc}:

In case $SC\_YE \leq max(SC\_Y1, SC\_Y2)$:

$$SSI\_PARPOS[3:0] \leq 15 - ceil(log2(max(SC\_Y1, SC\_Y2)))$$

In case $SC\_YE > max(SC\_Y1, SC\_Y2)$:

$$SSI\_PARPOS[3:0] \leq 15 - ceil(log2(SC\_YE))$$

The SSI shall sample a new angular value only after start-up or clock timing violation. TM is the minimum time required by the slave to realize that the data transmission is complete. It can be configured via SSI_TM. If the ECU triggers more than 16 clocks, without a clock violation, the last transmitted word is repeated.

In SSI mode a transfer timeout is represented with time Tm, and a transfer completion with time TP. Time TP is called the pause period, or the time delay between two consecutive clock sequences. Figure 10 illustrates the timing of the SSI signals. In Idle state, the encoder Data line remains at high level (a). After the first falling edge of SCLK, the position value of the encoder is held constant with the Data Level remaining at high level (a). Upon the first edge of SCLK, the MSB is transmitted, followed by the remaining bits. To indicate the correct end of transmission, the Data line must to be set to low level (c) after transmitting the LSB. After the timeout period ends, the encoder will update the position value, and the Data line will indicate a high level (d). The next transmission begins with the next sequence of SCLK pulses.

A Data line high level during the pause period T_P, following the timeout period T_m, requires a pullup resistor on the Data line, as shown in the recommended Example Application Diagrams in the datasheet.

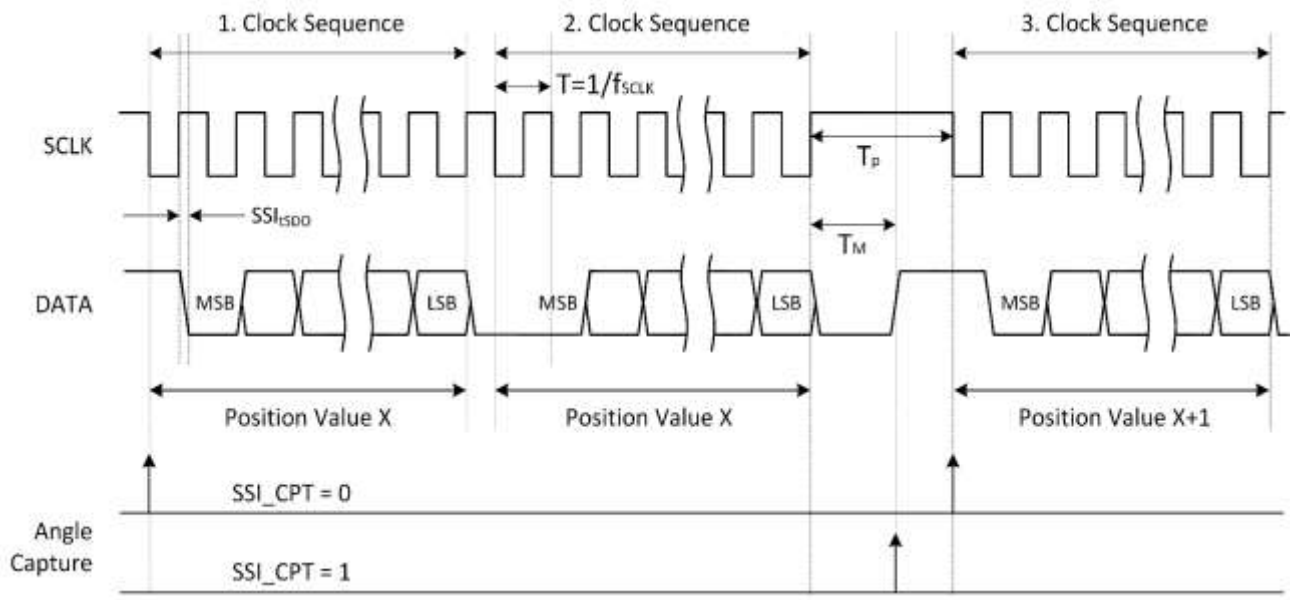

Figure 13: MLX90382 SSI Signal Timing Diagram

With the parameter **SSI_CPT**, either the falling edge on SCLK, or T_M can be selected for the angle acquisition. With **SSI_CPT** = 0, the falling edge on SCLK after start-up and the falling edge on SCLK after the pause pulse (T_P) is selected to trigger the angle acquisition. With **SSI_CPT** = 1, the angle acquisition is done after T_M passed. The SSI timeout T_M starts counting from the rising edge of the pause pulse (T_P). As the first timeout occurs after the first frame and not after start-up, the angle data of the first frame after start-up is invalid!
Note: For SSI clock frequencies above 2MHz SSI_CPT has to be set = 1!

6.7 Gain configuration

Table 18: NVRAM map – Gain Configuration Parameters

Field	Address	Bit	R/W	Description
AGC_GAIN_MIN	520 0x0208	[5:0]	R/W	AGC minimum gain, range [0...63
AGC_GAIN_MAX		[11:6]	R/W	AGC maximum gain, range [0...63]
-		[15:12]	NU	Not used

Definition

AGC_GAIN_MIN and **AGC_GAIN_MAX** are the limits in which the automatic gain control of the sensor can operate. These parameters can also be used to fix the gain by setting **AGC_GAIN_MIN = AGC_GAIN_MAX**. The range that one can fix or limit the gain is from 0 to 47. Default the gain range is set to the full range with **AGC_GAIN_MIN** = 0 and **AGC_GAIN_MAX** = 63.

6.8 Calibration- Sensitivity and Orthogonality Correction

Table 19: NVRAM map – Gain Configuration Parameters

Field	Address	Bit	R/W	Description
S_IQ	540 0x021C	[15:0]	R/W	Relative cross-sensitivity from in-phase to quadrature phase component, range is [-2^{15}, $+2^{15}$] which corresponds to a correction of [-1, +1]; overrides factory trimming, if non-zero.
S_QQ	542 0x021E	[15:0]	R/W	Relative sensitivity for quadrature component, range is [0, $+2^{16}$] which corresponds to a correction of [0, 2]; overrides factory trimming if non-zero.

Definition

S_QQ is the relative sensitivity for the quadrature component, range 0 to 2^{16} which corresponds to a correction of 0 to 2, used to calibrate the sensitivity mismatch between I and Q. **S_IQ** is the relative cross-sensitivity from in-phase to quadrature phase component, range -2^{15} to $+2^{15}$ which corresponds to a correction of -1 to +1, used to calibrate the orthogonality error of the sensor or system. If the values of these parameters are set to 0, meaning **S_IQ = 0x0000** and **S_QQ = 0x8000**, the factory trimmed settings are used for these parameters. The factory trimmed settings are selected in function of the selected **SENSING_MODE**.

6.8.1 Adaptive Loop Filter behaviour during calibration

For application scenarios such as off-axis or trough shaft application modes, the amplitude mismatch between the magnetic fields B_I and B_Q as seen by the sensor can go from a few percent for multi-pole pair magnets to 50% for single-pole pair magnets.

In the case of a larger amplitude mismatch between the magnetic fields B_I and B_Q, uncompensated GC_I and GC_Q could trigger the adaptive loop filter monitor, ALF. This phenomenon is automatically resolved after: the sensitivity mismatch calibration is performed to compensate GC_I and GC_Q for the amplitude mismatch, the orthogonality calibration is performed and/or 16-point linearization is performed.

To avoid that the DSP triggers an error on the ALF during the calibration, the diagnostic on the ALF, **DE_DSP_ALF**, should be disabled in the Diagnostic Configuration Parameters.

Note: The content of the Diagnostic Configuration Parameters will affect the safety hardware metrics and shall not be permanently disabled unless a proper impact analysis is conducted. For further information please refer to the MLX90382 Safety Manual.

Table 20: NVRAM map – Diagnostic Configuration Parameters

Field	Address	Bit	R/W	Description
DE_OV_VDD	602 0x025A	0	R/W	Disable VDD overvoltage error
DE_UV_VDD		1	R/W	Disable VDD undervoltage error
DE_OV_VDDD		2	R/W	Disable VDDD overvoltage for error
DE_VDDA		3	R/W	Disable VDDA over-/undervoltage error
DE_VAUX		4	R/W	Disable VAUX over-/undervoltage error
DE_AGC		5	R/W	Disable AGC error
DE_DSP		6	R/W	Disable DSP related errors
DE_RCO		7	R/W	Disable RCO monitor
DE_ADC_LIN		8	R/W	Disable ADC linearity error
DE_ADC		9	R/W	Disable ADC related errors
DE_ADC_OVF		10	R/W	Disable ADC overflow error
DE_AFE_REF		11	R/W	Disable AFE reference error
DE_TEMP		12	R/W	Disable over/under temperature error
DE_TEMP_MAX		13	R/W	Disable max temperature error
DE_SPEED		14	R/W	Disable speed error
DE_DSP_ALF		15	R/W	Disable DSP ALF error

6.8.2 Adaptive Loop Filter after calibration

In paragraph 6.8.1 we explained the I and Q mismatch has an impact on the behaviour of the Adaptive Loop Filter. A large mismatch in amplitude of the GC_I and GC_Q signals can be seen as a change in speed on which the ALF will act. This phenomenon is automatically resolved after the calibration is performed to compensate the GC_I and GC_Q mismatch. If a calibration is not desired because for example the target angle accuracy is not that critical, then the loop filter constant settings of the ALF need to be adapted.

The loop filter constants **DSP_LFC_LO** and **DSP_LFC_HI** define the possible range of Adaptive Loop Filter bandwidth adaption. Setting both to equal values disables the automated adaptation. The overshoot can be defined via **DSP_SROS**. For details see datasheet chapter “High-Dynamic Performance”.

In case the Sensitivity Mismatch Calibration is skipped and/or the remaining GC_I and GC_Q amplitude mismatch is large, the loop filter constants **DSP_LFC_LO** and **DSP_LFC_HI** need to be set to a larger bandwidth range. Please refer to the datasheet for more information on the range of the parameters.

Table 21: NVRAM map

Field	Address	Bit	R/W	Description
DSP_IQNEG	582 0x0246	[1:0]	R/W	I/Q sign inversion: Bit [0]: 0: GC_I, 1: -GC_I Bit [1]: 0: GC_Q, 1: -GC_Q
DSP_GC_AVG		[4:2]	R/W	GC averaging control: 0: Averaging off, 1…6: sum(k = 1…4^DSP_GC_AVG, $gc_{i/q}(k)$/4^DSP_GC_AVG) 7: sum(k = 1…8, $gc_{i/q}(k)$/8)
DSP_DRIFTC_DIS		5	R/W	Disable delay (drift) compensation
Reserved		6	R/W	Reserved, don’t change
DSP_LFC_LO		[10:8]	R/W	lowest DSP loop filter bandwidth; adaptive loop filter enabled, if DSP_LFC_LO < DSP_LFC_HI
DSP_LFC_HI		[13:11]	R/W	upper DSP loop filter bandwidth;
DSP_SROS		[15:14]	R/W	Phase tracking step response overshoot

6.8.3 Sensitivity Mismatch Calibration

The MLX90382 sensor has one parameter to calibrate the sensitivity mismatch between the two angle components, **S_QQ**. By default, **S_QQ** is used to compensate for the sensitivity mismatch between the in-phase to quadrature phase component of the sensor. But **S_QQ** can also be used to compensate for the amplitude mismatch of the field components of the applied magnetic fields.

For the calculation of the sensitivity mismatch one needs to measure the MIN and MAX level of the two angle components I/Q of the applied magnetic field, as seen by the sensor (marked in orange in the figure below). There are two techniques to obtain the measurements:

6.8.3.1 Absolute Positioning

With an absolute angle reference, four fix angles positioned at -90°, 0°, 90° and 180° are measured. For the measurement, an accurate reference angle is important to ensure that the actual MIN and MAX level is measured of **GC_I** and **GC_Q**.

6.8.3.2 Min-Max Tracking Via Data Acquisition

The DAQ technique searches for the MIN-MAX levels of the two I/Q signals. While the magnet turns the micro controller or DAQ setup keeps track of the I and Q signals and extracts the MIN and MAX level of **GC_I** and **GC_Q**.

The two angle components I/Q of the magnetic field, of an applied angle measured by the sensor, are stored in the **GC_I** and **GC_Q** register of the DSP, see chapter 7.2.4.

GC_I and **GC_Q** are filtered values. The applied filter setting in the sensor and acquisition speed of the SPI setup determines which rotation speed can be used to obtain the MIN-MAX levels of the two I/Q signals or vice versa. Additional filtering might be needed by taking the average MIN-MAX value of multiple rotations of the magnet.

Important: The measurement of **GC_I** and **GC_Q** needs to be done with **S_QQ = 2^{15} +1 = 0x8001 = 1** and **S_IQ = 0x0001**!
The AGC GAIN needs to be programmed to a fixed value, **AGC_GAIN_MIN = AGC_GAIN_MAX = 10.**
If needed the diagnostic on the ALF, **DE_DSP_ALF**, has to be disabled.

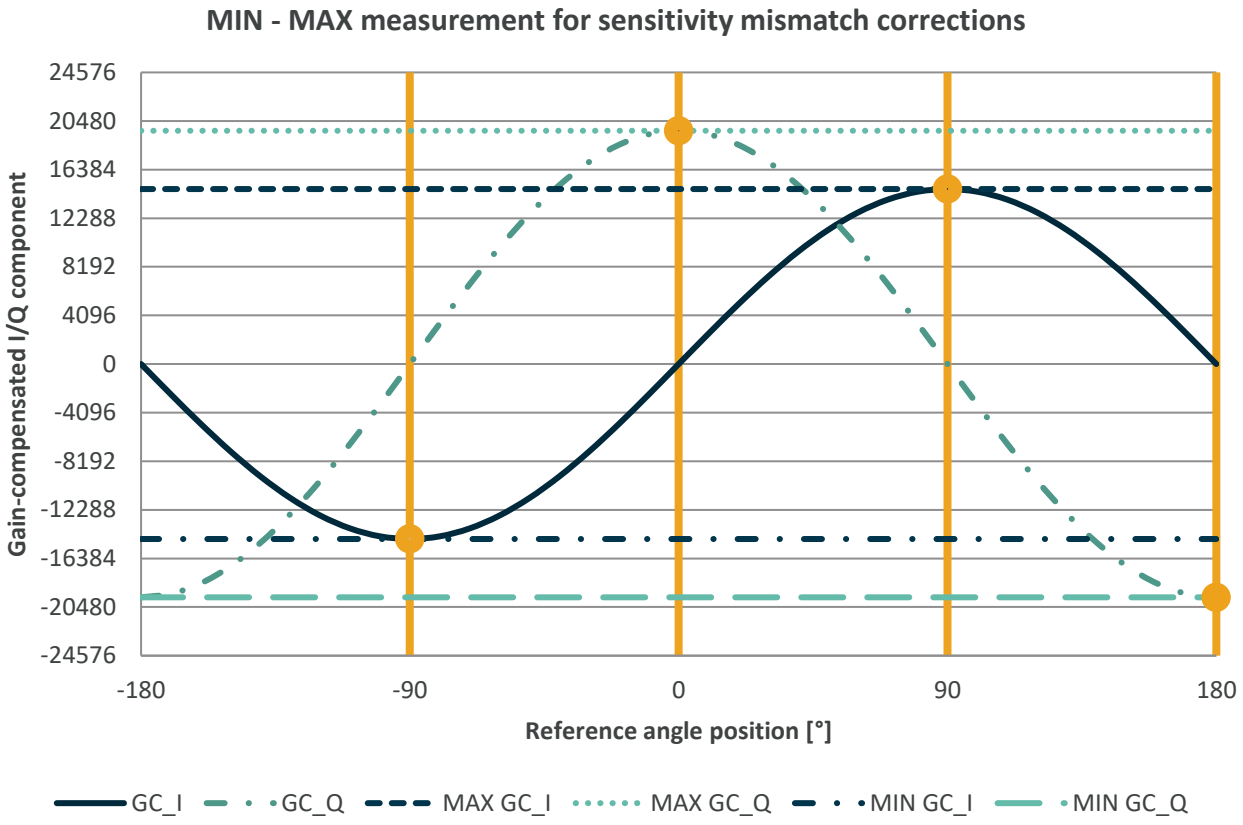

Figure 14: MIN - MAX measurement for I/Q sensitivity mismatch calibration method

6.8.3.3 Calculation

As described in chapter 7.2.3 I/Q measurements, the parameters **GC_I** and **GC_Q** are signed 2's complement values of 16bit. **S_QQ** is an unsigned 16bit value that corrects the relative sensitivity for the quadrature component with a range of 0 to 2. This parameter can be used to trim the sensitivity mismatch, with a range of 0.5 to 2. **S_QQ** can be recalculated with the MIN and MAX value of **GC_I** and **GC_Q**:

S_QQ sensitivity mismatch:

$$S\_QQ[15:0] = 2^{15} * \frac{GC\_I_{SPAN}}{GC\_Q_{SPAN}}$$

Where:

$$GC\_I_{SPAN}[signed] = GC\_I_{MAX}[signed] - GC\_I_{MIN}[signed]$$
$$GC\_Q_{SPAN}[signed] = GC\_Q_{MAX}[signed] - GC\_Q_{MIN}[signed]$$

6.8.4 Orthogonality Calibration

S_IQ is a signed 2's complement 16bit value that corrects the relative cross-sensitivity from in-phase to quadrature-phase component, the orthogonality error. The orthogonality errors β_IMC and β_Magnet can be corrected with the following method. The orthogonality error is calculated with the vector of two or four 90° shifted angle measurements from -135°, -45°, 45° and 135°. The method calculates the amplitude mismatch of the angel vector at -135°, -45°, 45° and 135°. The method is carried out **after** the Sensitivity Mismatch Calibration method is applied.

Important: The measurement of **GC_I** and **GC_Q** needs to be done with **S_IQ = 0x0001**!
The AGC GAIN needs to be programmed to a fixed value, **AGC_GAIN_MIN = AGC_GAIN_MAX = 10.**

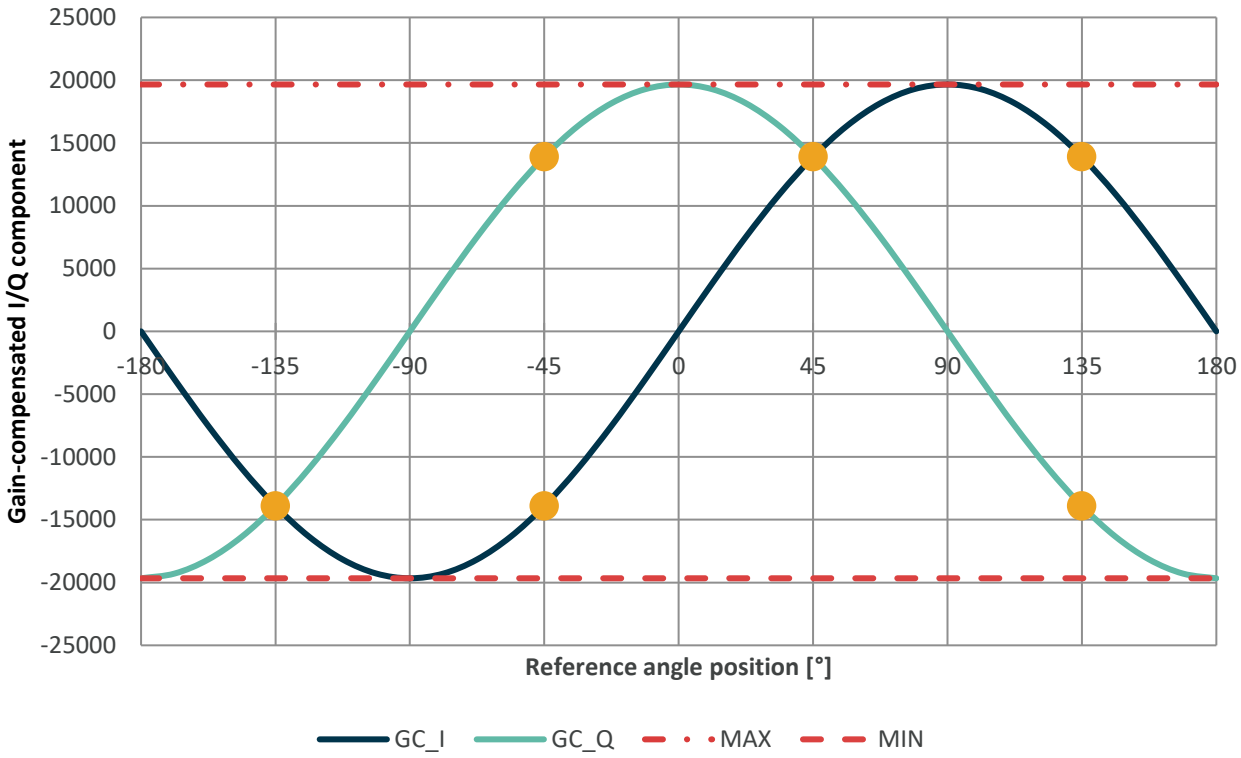

Figure 15: Eight measurements (four per output) for the orthogonality calibration method

There are two techniques to obtain the measurements.

6.8.4.1 Absolute Angle Reference

With an absolute angle reference, two or four fixed angles, positioned at -135°, -45°, 45° and 135° are measured. For the measurement, an accurate reference angle is important.

6.8.4.2 Relative Angle Reference

One can use the sensor's angle as a reference, after the sensitivity mismatch calibration method is applied for **S_QQ**. The sensitivity mismatch calibration method is important to ensure a reference angle as accurate as possible.

6.8.4.3 Calculation

Vectors:

$$V_{-135} = \sqrt{GC\_Q_{-135}{}^2 + GC\_I_{-135}{}^2}$$

$$V_{-45} = \sqrt{GC\_Q_{-45}{}^2 + GC\_I_{-45}{}^2}$$

$$V_{45} = \sqrt{GC\_Q_{45}{}^2 + GC\_I_{45}{}^2}$$

$$V_{135} = \sqrt{GC\_Q_{135}{}^2 + GC\_I_{135}{}^2}$$

Orthogonality error:

$$\beta = 2 \times atan2\left(\frac{V_{135} - V_{45}}{V_{135} + V_{45}}\right)$$

Or:

$$\beta = 2 \times atan2\left(\frac{(V_{135} + V_{-45}) - (V_{-135} + V_{45})}{(V_{135} + V_{-45}) + (V_{-135} + V_{45})}\right)$$

$$S\_IQ = 2^{15} \times 2 \times \left(\frac{(V_{135} + V_{-45}) - (V_{-135} + V_{45})}{(V_{135} + V_{-45}) + (V_{-135} + V_{45})}\right)$$

6.9 Self-Calibration - Sensitivity and Orthogonality Correction

Table 22: NVRAM map – Gain Configuration Parameters

Field	Address	Bit	R/W	Description
RMM_FAST	598 0x256	[2:0]	R/W	Settling configuration for Self-Calibration
RMM_LFC		[5:3]	R/W	Settling constant for the Self-Calibration tracking filter
RMM_AVG_MIN		[7:6]	R/W	Minimum value for Self-Calibration averaging
RMM_AVG_MAX		[9:8]	R/W	Maximum value for Self-Calibration averaging
Reserved		[14:10]	R/W	Reserved, don't change.
-		15	NU	Not used
RMM_ASQQ_MIN	600 0x258	[4:0]	R/W	Self-Calibration minimum ASQQ clamping value, ±6.25 %SMM/LSB
RMM_ASQQ_MAX		[9:5]	R/W	Self-Calibration maximum ASQQ clamping value, ±6.25 %SMM/LSB
RMM_ASIQ_MAX		[14:10]	R/W	Self-Calibration maximum absolute ASIQ clamping value, 0.7 %/LSB
Reserved		15	R/W	Reserved, don't change.
DE_AROC	604 0x025C	0	RW	Disable AROC error
DE_SR		[3:1]	RW	If 3, register monitor is disabled, else changes on other CEE_SREG fields are overwritten by corresponding NVRAM content within FDTI.
DE_DIE		4	RW	Disable Crack detection error
DE_INTP		5	RW	Disable INTP errors
DE_SCXY		6	RW	Disable SCXY errors
DE_DSP_RMM		[8:7]	RW	Disable Residual mismatch correction: Bit[1] - disable adaptive orthogonality correction Bit[0] - disable adaptive sensitivity correction
Reserved		9	RW	Reserved = 1, don't change.
-		[14:10]	NU	Not used
EH_WD_EN		15	RW	If 1, warm reset is issued after 15ms in Hi-Z safe state
RMM_ASIQ	98 0x062	[15:0]	R	Adaptive orthogonality correction value AS_IQ
RMM_ASQQ	100 0x064	[15:0]	R	Adaptive sensitivity correction value AS_SQ

Definition

The MLX90382 provides a self-calibration algorithm to correct the sensitivity and orthogonality error of the sensor.
The RMM (Residual Mismatch Measurement) continuously measures residual sensitivity (gain) mismatch and/or orthogonality (phase) mismatch and adapts digital corrections **RMM_ASIQ** and/or **RMM_ASQQ** accordingly.

The RMM is enabled by the parameter **DE_DSP_RMM**. The adaptive orthogonality correction and adaptive sensitivity correction can be enabled independently. The RMM can be enabled temporarily for the End of Line calibration of the **S_QQ** and **S_IQ** parameters, enabled permanently for compensating the lifetime drift of the sensor or a combination of both.

Same as for the **S_QQ, RMM_ASQQ** is the relative sensitivity for the quadrature component, range 0 to 2^{16} which corresponds to a correction of 0 to 2, used to calibrate the sensitivity mismatch between I and Q. Same as for the **S_IQ, RMM_ASIQ** is the relative cross-sensitivity from in-phase to quadrature phase component, range -2^{15} to $+2^{15}$ which corresponds to a correction of -1 to +1, used to calibrate the orthogonality error of the sensor or system. The amount in which the RMM can change the **RMM_ASQQ** and **RMM_ASIQ** is set by the **RMM_ASQQ_MIN**, **RMM_ASQQ_MAX** and **RMM_ASIQ_MAX**. These parameters are 5 bits parameters with a resolution of ±6.25 %SMM/LSB for **RMM_ASQQ_MIN** and **RMM_ASQQ_MAX** leading to a full range of 0 to 2 and 0.7 %/LSB for **RMM_ASIQ_MAX** leading to an absolute rage of 0 to 0.224.

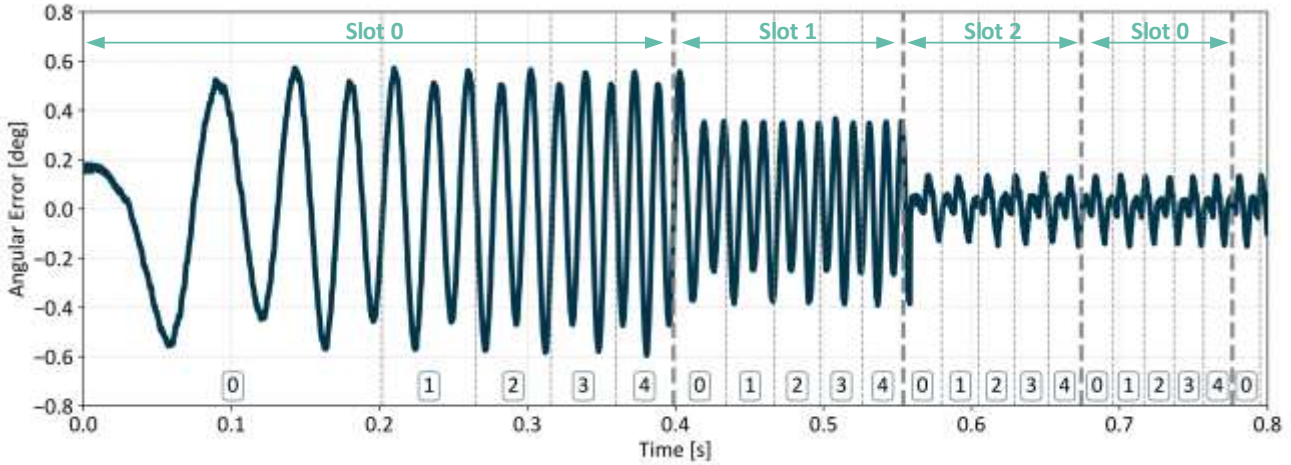

Figure 16: Example illustration of the angle error correction of the self-calibration method

The RMM uses the same technique as described in the sections Sensitivity Mismatch Calibration and Orthogonality Calibration.

In short:
Slot: **RMM_AVG_MIN** and **RMM_AVG_MAX** control the averaging, the number of 450° electrical rotations that are used to measure and calculate the new **RMM_ASIQ** and **RMM_ASQQ** correction parameters.
Settling speed: **RMM_FAST** controls the settling speed of the filter at start-up.
Filtering: **RMM_LFC** controls the smoothing factor of the IIR filter. **RMM_ASQQ_MIN**, **RMM_ASQQ_MAX** and **RMM_ASIQ_MAX** define the boundaries of the filter.

The table above lists 4 scenarios to quickly configure the self-calibration of the sensor. The following chapters further explain the working of the self-calibration.

Table 23: Customer Scenarios to use the self-calibration

Customer scenario	Goal	DSP_RMM_AVG_MIN / DSP_RMM_AVG_MAX	RMM_LFC_MAX (steady)	DSP_RMM_FAST (start-up)
EoL calibration – quick convergence	Converge fast; angle jumps acceptable at EoL	MIN=0 / MAX=1 (≈5 to 20 electrical rotations per slot)	2	4–6
In operation – high speed, clean signal	Track drift with good noise immunity	MIN=0 / MAX=3 (≈5 to 320 electrical Rotations per slot)	4–5	0 to 4
In operation – vibration / EMI-noisy	Max robustness; slow but steady	MIN=0 / MAX=3 (≈5 to 320 electrical Rotations per slot)	6–7	0 to 1
Start–stop duty (frequent power cycles)	Quick re-settle without jumps	MIN=1 / MAX=2 (≈20 to 320 electrical Rotations per slot)	5–6	0–1

6.9.1 Angular Range for Averaging Control (AVG)

To keep the estimates of the residual error of the sensitivity/orthogonality within a target angle, the device increases the number of angular ranges it averages in function of the signal noise. In the beginning of SLOT 0, the device sets the amount of necessary angular ranges (number of 450° electrical rotations) for each SLOT based on the current signal noise. According to the current signal noise the internal register RMM_AVG is set. RMM_AVG can be clamped by the customer using **DSP_RMM_AVG_MIN** and **DSP_RMM_AVG_MAX**. With this, one can control the min and max range of rotations that are required for the application

Table 24: Self calibration filter sampling settings in function of the set AGC

RMM_AVG	Number of 450° electrical rotations
0	5
1	20
2	80
3	320

6.9.2 Loop Filter Control (LFC)

At power on the sensor loads the **S_QQ** and **S_IQ** parameters from the NVRAM for compensation of the sensitivity mismatch SC_QQ and orthogonality SC_IQ. When the self-calibration **DE_DSP_RMM** is enabled the SC_QQ and/or SC_IQ are adapted with the **RMM_ASQQ** adaptive sensitivity correction and **RMM_ASIQ** adaptive orthogonality correction.

The adaptation is done via a 1-pol IRR with a smoothing factor $\alpha = \frac{1}{RMM\_LFC}$. The factor is set by the parameter **RMM_LFC_MAX** where $RMM\_LFC = 2^{RMM\_LFC\_MAX}$.
The table below lists the range of the smoothing factor.

Table 25: Filter smoothing factor

RMM_LFC_MAX[2:0]	$RMM\_LFC = 2^{RMM\_LFC\_MAX}$	$\alpha = \frac{1}{RMM\_LFC}$
0	1	1
1	2	0.5
2	4	0.25
3	8	0.125
4	16	0.0625
5	32	0.03125
6	64	0.015625
7	128	0.0078125

Guide for choosing the right values of RMM_LFC_MAX

Choose **RMM_LFC_MAX** in function of noise vs. tracking trade-off (steady state). In a noisy environment choose a larger **RMM_LFC_MAX** to have a low ripple on the angle error. For a more agile application choose smaller **RMM_LFC_MAX**. It is always recommended to keep **RMM_LFC_MAX** as large as possible.

6.9.3 Fast Settling control (FAST)

The **DSP_RMM_FAST** register controls the settling behaviour after start-up of the IC. It sets how many initial RMM update cycles run in “fast” mode before switching to the steady, low-noise IIR set by the **RMM_LFC_MAX**.
A small counter that holds the loop in a fast mode for the first N valid updates, then switches to the steady-state mode set by **RMM_LFC_MAX**.

During this fast window, the implementation uses a much larger step (effectively RMM_LFC=2, and in some cases DSP_RMM_FAST, RMM_LFC=1). With this the IIR filter settles much faster.
It determines how many early updates are “aggressive” before handing off to the slow, quiet tracking.

⚠ In case RMM_LFC=1, the update is very aggressive and could cause a safe state due to DIAG_ALF as it is seen as a high acceleration. This depends on the initial error for sensitivity and orthogonality. Note that the DSP_RMM_FAST also controls the RMM_LFC setting and has therefore also an impact.

Table 26: Fast Settling control

DSP_ RMM_ FAST	Count of first cycle at RMM_LFC=1	Count of cycles with RMM_LFC=2	Update cycles until steady state with $RMM\_LFC = 2^{RMM\_LFC\_MAX}$	Notes	Recommendation
0	0	0	immediate	Slowest settling at start-up	in-operation
1	0	1	1	One quick correction, then steady.	in-operation
2	0	2	2	Two quick corrections, then steady	in-operation
3	0	3	3	Three quick corrections, then steady	in-operation / EoL
4	1	3	4	Uses very aggressive first correction, then 3 quick once. For large initial errors. (DEFAULT)	EoL
5	2	3	5	Uses very aggressive first correction, then 4 quick once. For large initial errors	EoL
6	3	3	6	Very aggressive. Check for overshoot (due to noise).	EoL
7	4	3	7	Max fast window. ⚠To be used with caution.	EoL

The following 2 figures show a normal angle error reduction in-operation and a fast angle error reduction for End of Line calibration. The plots show the angle error reduction when the application is powered on.
The measurement was done with a NdFeB disc magnet with a diameter of 10mm and a height of 5mm at 1000RPM in an end of shaft setup.

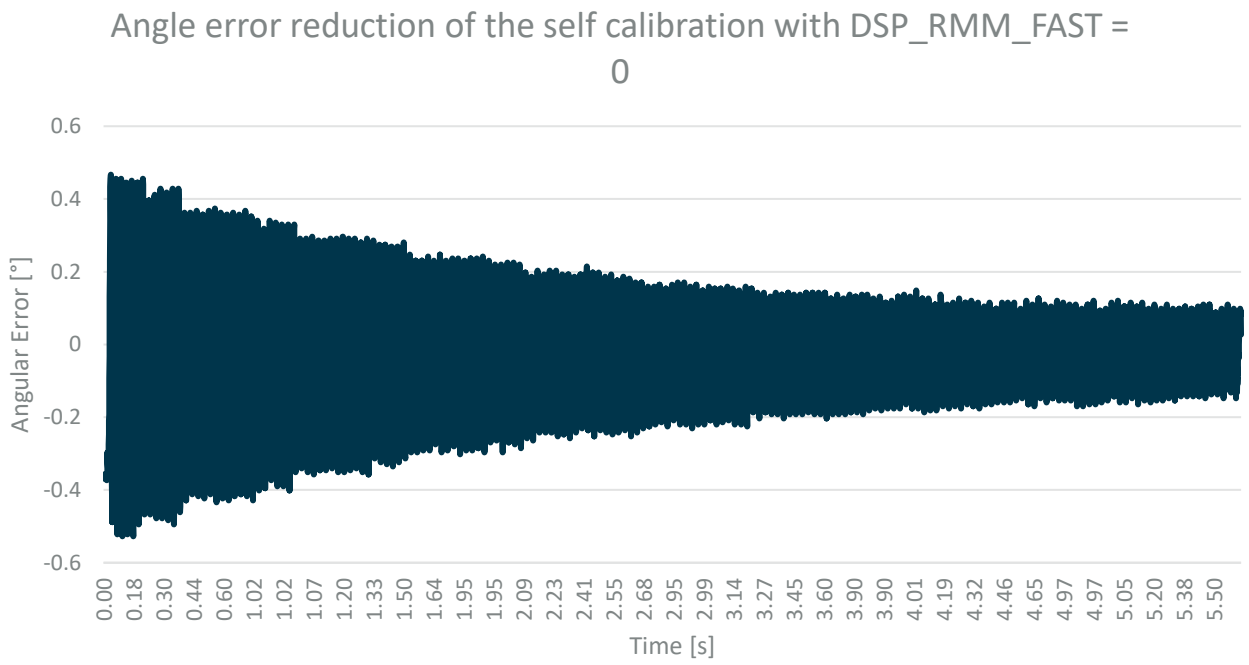

Figure 17: Example illustration of the angle error correction of the self-calibration method with DSP_RMM_FAST = 0 for in-operation use

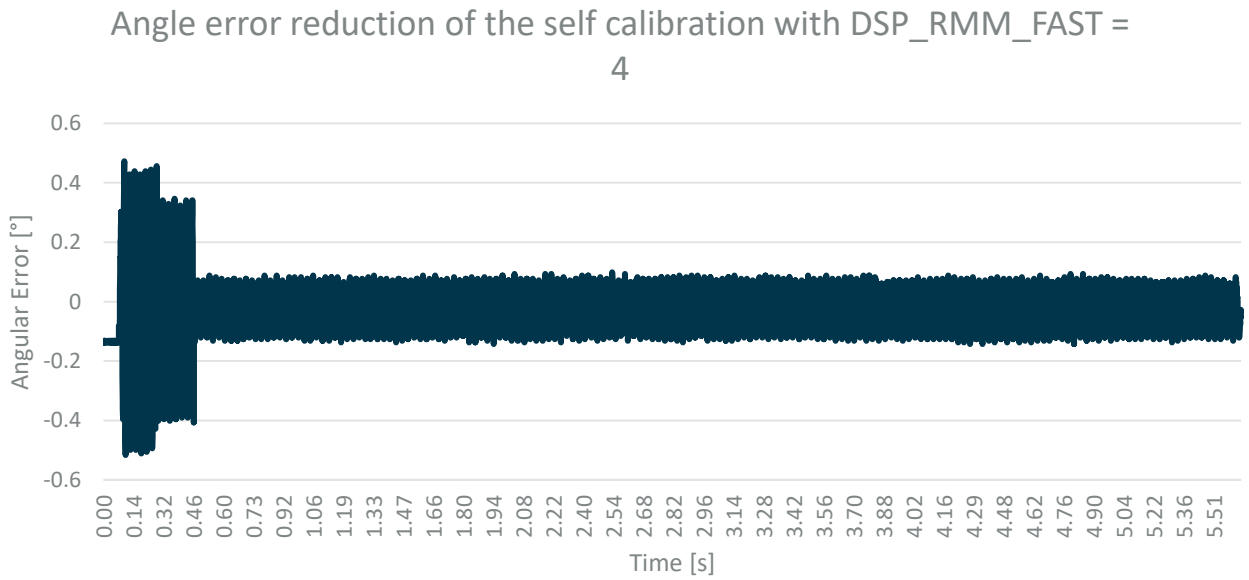

Figure 18: Example illustration of the angle error correction of the self-calibration method with DSP_RMM_FAST = 4 for End of Line calibration

6.10 End-of-line calibration using the self-calibration function

The customer can save the result of AS_QQ and AS_IQ to the NVRAM. This is a scenario during end-of-line calibration to save the current status of compensation.

The internal gain and orthogonality compensation in the DSP using the RMM is as follows:

$$\begin{bmatrix} gc\_i \\ gc\_q \end{bmatrix} = M \cdot \begin{bmatrix} dmux\_i \\ dmux\_q \end{bmatrix}$$

with

$$M = \begin{bmatrix} 1 & AS\_IQ/2^{15} \\ (AS\_IQ - SC\_IQ)/2^{15} & AS\_QQ/2^{15} \end{bmatrix}$$

One might store the result of the compensation by updating the register S_IQ and S_QQ. For this an upper triangle matrix needs to be calculated based on the compensation matrix R to achieve the following result

$$\widetilde{M} = \begin{bmatrix} 1 & SC\_IQ_{new}/2^{15} \\ 0 & SC\_QQ_{new}/2^{15} \end{bmatrix}$$

$$\begin{bmatrix} gc\_i \\ gc\_q \end{bmatrix} = \begin{bmatrix} 1 & SC\_IQ_{new}/2^{15} \\ 0 & SC\_QQ_{new}/2^{15} \end{bmatrix} \cdot \begin{bmatrix} dmux\_i \\ dmux\_q \end{bmatrix}$$

Two possible methods can be used:

1) Q-R decomposition of the matrix R, so called as Gramm-Schmidt method.

Compute an orthonormal basis Q and an upper-triangular matrix R such that M ≈ Q·R using the (classical) Gram–Schmidt process.

2) A direct calculation of the Q-R decompensation for the elements of R in a closed form:

The calculation assumes that all parameters are normalised by 2^15:
e.g.

$$AS\hat{}IQ = \frac{AS\_IQ}{2^{15}} \qquad AS\hat{}QQ = \frac{AS\_QQ}{2^{15}} \qquad SC\hat{}IQ = \frac{S\_IQ}{2^{15}} \qquad SC\hat{}QQ = \frac{S\_QQ}{2^{15}}$$

$$SC\_IQ_{new} = \frac{AS\hat{}IQ + (AS\hat{}IQ - SC\hat{}IQ).AS\hat{}QQ}{1 + (AS\hat{}IQ - SC\hat{}IQ)^2} . 2^{15}$$

$$SC\_QQ_{new} = \frac{AS\hat{}QQ - (AS\hat{}IQ - SC\hat{}IQ).AS\hat{}IQ}{\sqrt{1 + (AS\hat{}IQ - SC\hat{}IQ)^2}} . 2^{15}$$

The values SC_IQ_{new} and SC_QQ_{new} can be stored in **S_IQ** and **S_QQ.**

The QR-based decomposition removes an orthogonal rotation of angle and with this introduces a constant angular error offset that can be calculated by:

$$\Delta\varphi = -arctan\left(\frac{AS_{IQ} - SC\_IQ}{2^{15}}\right)$$

6.11 16-Point linearization

Table 27: NVRAM map - 16-Point Linearization Configuration Parameters

Field	Address	Bit	R/W	Description
PEQ_GAIN	522 0x020A	[2:0]	R/W	Linearization gain. If > 0, phase offsets per reference point angle are POFSxx[15:0] = signed(PEQxx) * 2^(PEQ_GAIN-1), else 0
-		[15:3]	NU	Not used
PEQ00	524 0x020C	[7:0]	R/W	Phase Equalizer value at 0/16 * 360°
PEQ01		[15:8]	R/W	Phase Equalizer value at 1/16 * 360°
PEQ02	526 0x020E	[7:0]	R/W	Phase Equalizer value at 2/16 * 360°
PEQ03		[15:8]	R/W	Phase Equalizer value at 3/16 * 360°
PEQ04	528 0x0210	[7:0]	R/W	Phase Equalizer value at 4/16 * 360°
PEQ05		[15:8]	R/W	Phase Equalizer value at 5/16 * 360°
PEQ06	530 0x0212	[7:0]	R/W	Phase Equalizer value at 6/16 * 360°
PEQ07		[15:8]	R/W	Phase Equalizer value at 7/16 * 360°
PEQ08	532 0x0214	[7:0]	R/W	Phase Equalizer value at 8/16 * 360°
PEQ09		[15:8]	R/W	Phase Equalizer value at 9/16 * 360°
PEQ10	534 0x0216	[7:0]	R/W	Phase Equalizer value at 10/16 * 360°
PEQ11		[15:8]	R/W	Phase Equalizer value at 11/16 * 360°
PEQ12	536 0x0218	[7:0]	R/W	Phase Equalizer value at 12/16 * 360°
PEQ13		[15:8]	R/W	Phase Equalizer value at 13/16 * 360°
PEQ14	538 0x021A	[7:0]	R/W	Phase Equalizer value at 14/16 * 360°
PEQ15		[15:8]	R/W	Phase Equalizer value at 15/16 * 360°
PHASE_OFS	544 0x0220	[15:0]	R/W	Phase/Angle offset before signal conditioning, resolution 360°/2^16 (signed 2's-complement)

Definition

The 16-Point Linearization feature allows for equalizing angular deviations caused by asymmetries in the sensor system consisting of the magnet and the sensor IC. The 16 signed equalization values **PEQ00** to **PEQ15** characterize an angular error curve at angular sample points of 360°/16*[00 … 15]. All intermediate values are linearly interpolated, as shown in Figure 19. After equalization, the residual error curve is the difference between the input error curve and the interpolated equalization curve.

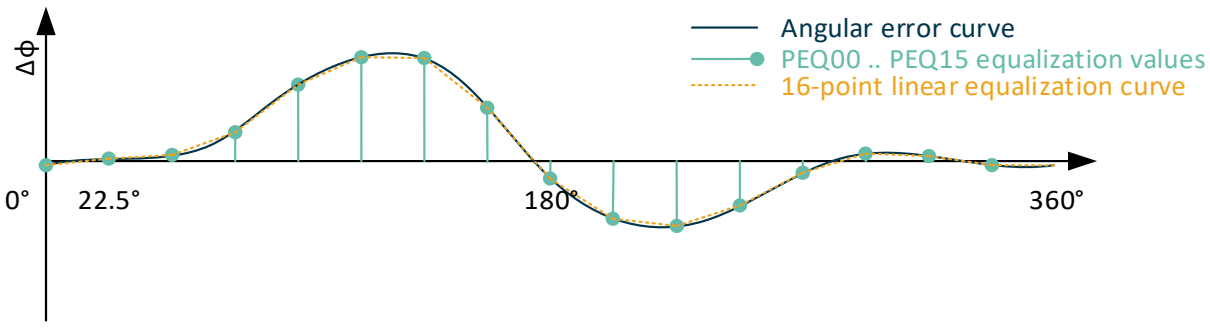

Figure 19: 16-point linearization of angular error curve

The angular error curve should be measured with quasi-static or low constant speed rotation. As the rotational speed increases, the 16-point Linearization feature automatically adapts to the low-pass band limitation of the error curve.
The equalization strength versus resolution can be adjusted depending on the value of **PEQ_GAIN**. If **PEQ_GAIN** is set to 0, no equalization is applied. For **PEQ_GAIN** = [1 ... 7] the error curve is adjusted per sample point as:

$$\Delta\varphi(xx) = singed(PEQxx) * 2^{PEQ\_GAIN-17} * 360\ [°]$$

The signed equalization values **PEQ00** to **PEQ15** each have a range of -127 to 127. “Table 23: Equalization range and resolution per sample point for PEQ_GAIN” in the datasheet shows the equalization range and resolution per sample point.

As a final complement, the mechanical position of the magnet resulting in zero output value can be adjusted by setting the field **PHASE_OFS**. The value of this field is systematically added to the position value calculated by the phase tracking loop.

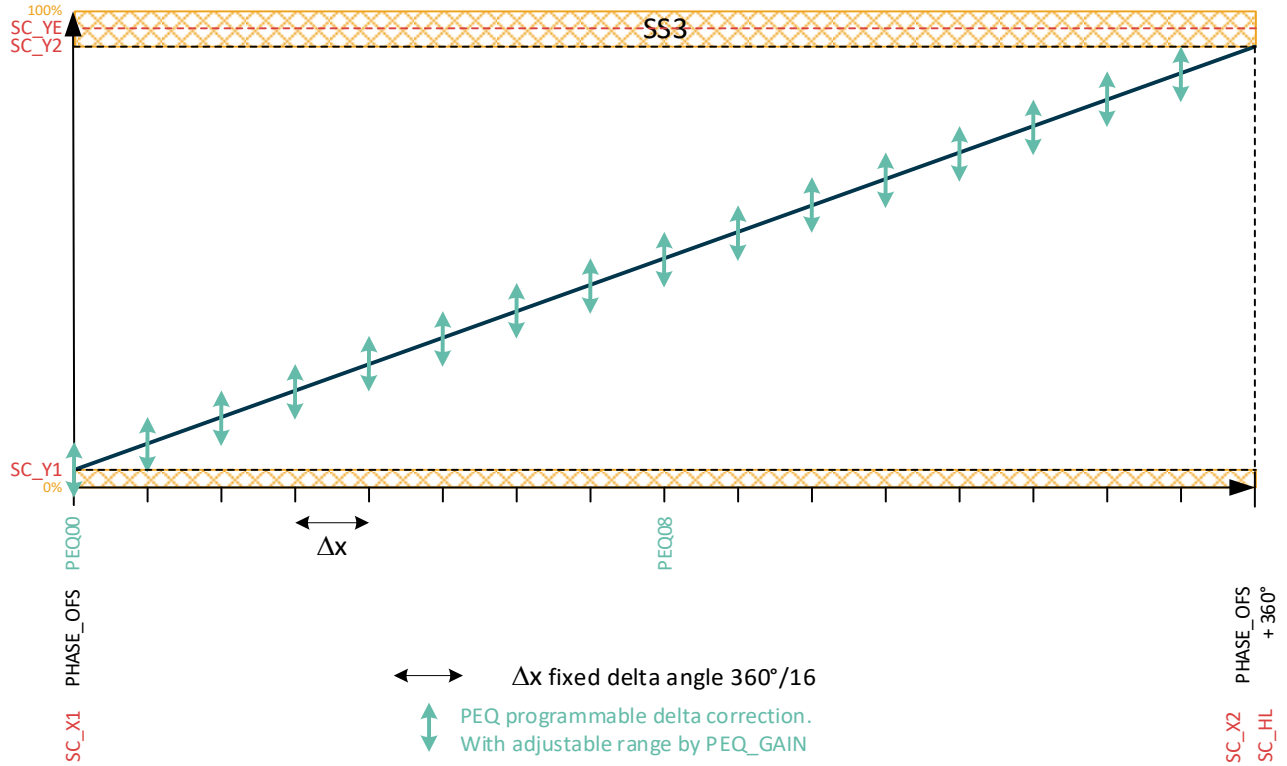

Figure 20: 360° application with 16-point linearization and signal conditioning

6.12 Signal conditioning

Table 28: NVRAM map - Signal Conditioning - Clamping Levels

Field	Address	Bit	R/W	Description
SC_X1	546 0x0222	[15:0]	R/W	Signal conditioning: X1, input range low, not applicable for the ABA
SC_X2	548 0x0224	[15:0]	R/W	Signal conditioning: X2, input range high, not applicable for the ABA
SC_Y1	550 0x0226	[15:0]	R/W	Signal conditioning: Y1, output range low
SC_Y2	552 0x0228	[15:0]	R/W	Signal conditioning: Y2, output range high
SC_YE	554 0x022A	[15:0]	R/W	Signal conditioning: output fault band level in SS3, if min(SC_Y1, SC_Y2) ≤ SC_YE ≤ max (SC_Y1, SC_Y2), SS3 changes to SS1 (OUT to Hi-Z).
SC_HL	556 0x022C	[7:0]	R/W	Signal conditioning: Transition point for clamping high to clamping low as offset from centre point of X range. Resolution 360°/2^8.
-		[15:8]	NU	Not used

Definition

The signal conditioning parameters **SC_X1** and **SC_X2** limit the angle range reported by the sensor. **SC_Y1** and **SC_Y2** define the output range in which the angle is reported, clamp high and low. These levels need to be adapted to the resolution of the selected output protocol. See Table 23: Example settings for SC. **SC_HL** defines the transition point for clamping high to clamping low as offset from the centre point of X range. Resolution 360°/2^8. **SC_YE** is the output level set to report a SS3 diagnostic fault. **SC_YE** is typically set outside the **SC_Y1** to **SC_Y2** range. If **SC_YE** is set within the **SC_Y1** to **SC_Y2** range, a SS3 diagnostic fault is reported in the same way as a SS1 diagnostic fault, OUT to Hi-Z. See the safety manual for a detailed explanation.

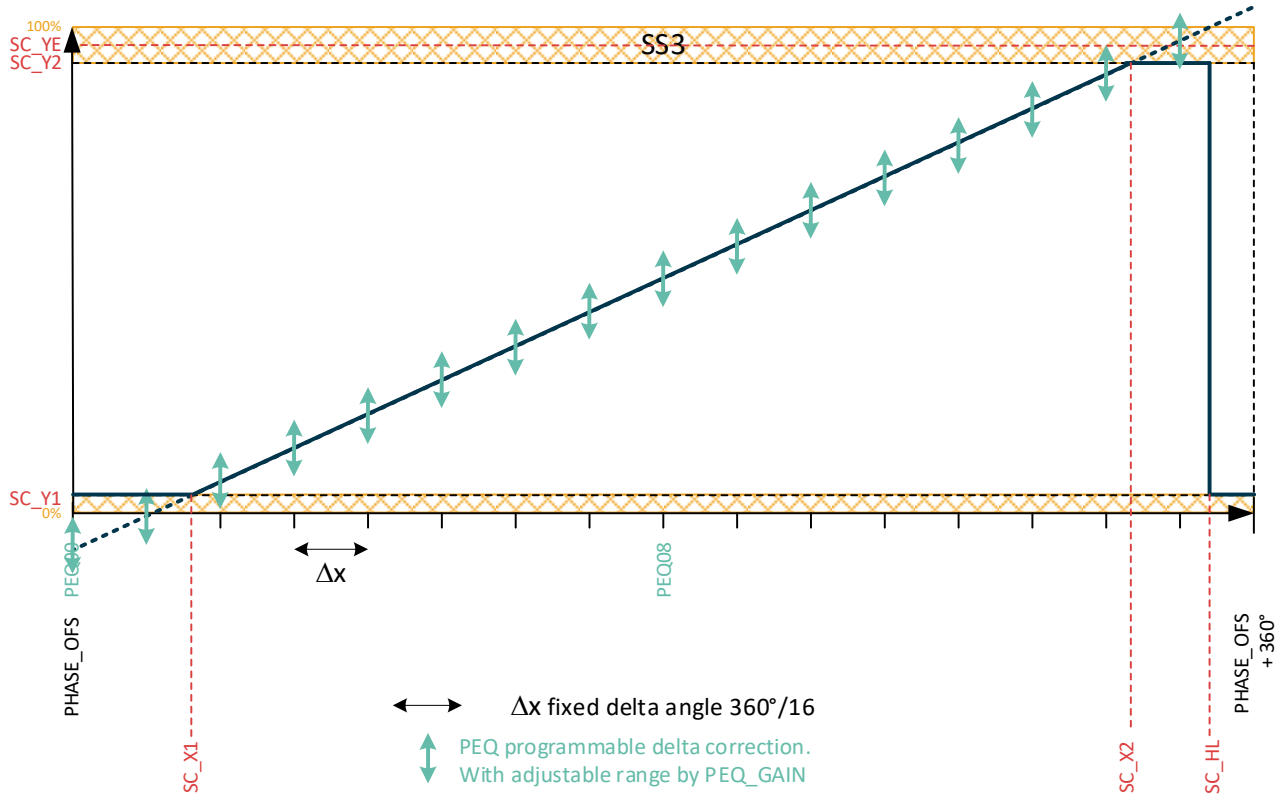

Figure 21: Limited angle range with 16-point linearization and signal conditioning

With this, the resolution of the angle after signal conditioning $\Delta\varphi_{sc}$ can be calculated by:

$$\Delta\varphi_{sc}[deg.] = \frac{360}{2^{16}} * ma\left(1, \frac{2^{16}-1}{|SC_{Y2} - SC_{Y2}|}\right)$$

Table 29: Example settings for SC

Parameter \ Protocol	SPI	SSI No Parity	SSI Parity	PWM	Comment
	2^{16}	2^{16} (SSI_PARPOS>8)	2^{15} (SSI_PARPOS=0)	2^{12}	Resolution
SC_Y1	0x0001	0x0001	0x0001	0x0052 (2%DC)	
SC_Y2	0xFFFD	0xFFFD	0x7FFD	0x0FAD (98%DC)	
SC_YE	0xFFFE	0xFFFE	0x7FFE	0x0FD6 (99%DC)	Outside SC_Y1-Y2 range
SC_X1	0x0000	0x0000	0x0000	0x0000	Full Angle range
SC_X2	0x0000	0x0000	0x0000	0x0000	
SC_HL	0x0080	0x0080	0x0080	0x0080	End of the angle range

6.13 DSP configuration

Table 30: NVRAM map

Field	Address	Bit	R/W	Description
DELAY_CUS	580 0x0244	[7:0]	R/W	Customer processing delay, range [0:255]*26/64/f_{RCO}
-		[15:8]	NU	Not used
DSP_IQNEG	582 0x0246	[1:0]	R/W	I/Q sign inversion: Bit [0]: 0: GC_I, 1: -GC_I Bit [1]: 0: GC_Q, 1: -GC_Q
DSP_GC_AVG		[4:2]	R/W	GC averaging control: 0: Averaging off, 1…6: sum(k = 1...4^DSP_GC_AVG, $gc_{i/q}$(k)/4^DSP_GC_AVG) 7: sum(k = 1...8, $gc_{i/q}$(k)/8)
DSP_DRIFTC_DIS		5	R/W	Disable delay (drift) compensation
Reserved		6	R/W	Reserved, don't change
DSP_LFC_LO		[10:8]	R/W	lowest DSP loop filter bandwidth; adaptive loop filter enabled, if DSP_LFC_LO < DSP_LFC_HI
DSP_LFC_HI		[13:11]	R/W	upper DSP loop filter bandwidth;
DSP_SROS		[15:14]	R/W	Phase tracking step response overshoot

Definitions

6.13.1 I/Q measurements

DSP_IQNEG sets the sign of the I and Q signals of the magnetic angle. The parameter can be used to match the orientation of the dual die TSSOP package or the intrinsic CW/CCW turn of the angle.

DSP_GC_AVG sets the averaging control of the gain compensated I and Q signals of the DSP. The averaging control suppresses noise and minimizes interface transactions for averaged measurements. The outputs gc_i[15:0] and gc_q[15:0] of the relative sensitivity correction shall be readable via R/O registers **DSP_GC_I** and **DSP_GC_Q**. These registers are intended for relative sensitivity and offset calibration.
With **DSP_GC_AVG**=0, reading **DSP_GC_I** shall latch the value in **DSP_GC_Q** until it was read as well.
With **DSP_GC_AVG**=[1...6], **DSP_GC_I** and **DSP_GC_Q** shall reflect the result of an averaging per channel of 4, 16, 64, 256, 1024 or 4096 samples.
With **DSP_GC_AVG**=7, **DSP_GC_I** and **DSP_GC_Q** shall reflect the result of an averaging per channel of 8 samples.
The averaging shall be restarted upon change on **DSP_GC_AVG** or after each read access on **DSP_GC_Q**.

6.13.2 Delay Compensation and Zero Position Adjustment

The speed signal provided by the phase tracking loop is used to compensate for phase errors due to the system latency, while the acceleration signal is used to compensate for phase errors during acceleration due to the latency of the speed calculation. Disabling the compensation can be done by setting the field **DSP_DRIFTC_DIS** for speed compensation.
The user furthermore disposes of the programmable field **DELAY_CUS**, to compensate for additional delays associated to e.g. filter networks in between the IC and the ECU, in steps of $(26/64)/f_{RCO}$.

6.14 Diagnostics

The content of the following register will affect the safety hardware metrics and shall not be modified unless a proper impact analysis is conducted. For further information please refer to the MLX90382 Safety Manual.

Table 31: NVRAM map – Diagnostic Configuration Parameters

Field	Address	Bit	R/W	Description
ABI_CFG	514 0x0202	[4:0]	R/W	ABI output driver configuration [13:11] driver strength, see section 6.1.1 [15:14] driver-mode: 0: off, 1: open-drain p-MOS, 2: open-drain n-MOS, 3: push-pull.
EH_MIN_SS_PERIOD		[7:5]	R/W	Minimum safe state period. Please refer to the MLX90382 safety manual for details.
-		[15:8]	NU	Not used
SC_YE	554 0x22A	[15:0]	R/W	Signal conditioning: Protocol fault band value in SS3
DIAG_TEMP_THD_LO	586 0x24A	[7:0]	R/W	Temperature threshold for under-temperature diagnostic, unit 2*[K]
DIAG_TEMP_THD_HI		[15:8]	R/W	Temperature threshold for over-temperature diagnostic, unit 2*[K]
DIAG_SPEED_THD	590 0x24E	[7:0]	R/W	Speed monitoring limit
DIAG_ALF_THD		[10:8]	R/W	Phase tracking error limit
-		[15:11]	NU	Note used
DIAG_AGC_THD_LO	594 0x252	[7:0]	R/W	AGC monitoring limit (lower bound)
DIAG_AGC_THD_HI		[15:8]	R/W	AGC monitoring limit (upper bound)
DE_OV_VDD	602 0x025A	0	R/W	Disable VDD overvoltage error
DE_UV_VDD		1	R/W	Disable VDD undervoltage error
DE_OV_VDDD		2	R/W	Disable VDDD overvoltage for error
DE_VDDA		3	R/W	Disable VDDA over-/undervoltage error
DE_VAUX		4	R/W	Disable VAUX over-/undervoltage error
DE_AGC		5	R/W	Disable AGC error
DE_DSP		6	R/W	Disable DSP related errors
DE_RCO		7	R/W	Disable RCO monitor
DE_ADC_LIN		8	R/W	Disable ADC linearity error
DE_ADC		9	R/W	Disable ADC related errors
DE_ADC_OVF		10	R/W	Disable ADC overflow error
DE_AFE_REF		11	R/W	Disable AFE reference error
DE_TEMP		12	R/W	Disable over/under temperature error
DE_TEMP_MAX		13	R/W	Disable max temperature error
DE_SPEED		14	R/W	Disable speed error
DE_DSP_ALF		15	R/W	Disable DSP ALF error
DE_AROC	604 0x025C	0	RW	Disable AROC error
DE_SR		[3:1]	RW	If 3, register monitor is disabled, else changes on other CEE_SREG fields are overwritten by corresponding NVRAM content within FDTI.
DE_DIE		4	RW	Disable Crack detection error
DE_INTP		5	RW	Disable INTP errors
DE_SCXY		6	RW	Disable SCXY errors
DE_DSP_RMM		[9:7]	RW	Disable Residual mismatch correction: Bit[1] - disable adaptive orthogonality correction Bit[0] - disable adaptive sensitivity correction
-		[14:10]	NU	Not used
EH_WD_EN		15	RW	If 1, warm reset is issued after 15ms in Hi-Z safe state

7 Register Map

7.1 EH_MST

Table 32: EH_MST register map

Field	Address	Bit	R/W	Description
ER_OV_VAUX	46 0x002E	15	R	Overvoltage on VAUX (auxiliary supply)
ER_OV_VDDD		14	R	Overvoltage on VDDD (digital Supply)
ER_OV_VDDA		13	R	Overvoltage on VDDA (analogue Supply)
ER_NVM_SR		12	R	Shadow register monitor error
ER_TEMP_HI		11	R	Over-temperature with regard to DIAG_TEMP_THR_HI
ER_TEMP_LO		10	R	Under-temperature with regard to DIAG_TEMP_THR_LO
ER_SPEED_HI		9	R	Trackaxis speed error
ER_AGC_HI		8	R	AGC monitoring limit (upper bound) triggered
ER_AGC_LO		7	R	AGC monitoring limit (lower bound) triggered
ER_ADC		6	R	ADC related errors
ER_ADC_LIN		5	R	ADC linearity error
ER_AFE_REF		4	R	AFE reference error
ER_DSP_ALF		3	R	DSP adaptive loop filter error
ER_DSP_TA		2	R	DSP trackaxis error
ER_DSP		1	R	DSP related error
ER_AROC		0	R	AROC error
-	48 0x0030	[15:10]	R	Not used
ER_SCXY		9	R	SCXY error
ER_INTP		8	R	INTP error
ER_DIE		7	R	Die crack detection
ER_TEMP_MAX		6	R	Over-temperature with regard to DIAG_TEMP_THR_MAX
ER_UV_VAUX		5	R	Undervoltage on VAUX
ER_UV_VDDA		4	R	Undervoltage on VDDA (analogue supply)
ER_UV_VDD		3		Undervoltage on external supply
ER_NVM_CRC		2		NVRAM CRC error
ER_NVM_DED		1		NVRAM double bit error
DIAG_AMP_ADC	50 0x0032	[15:8]	R	Signal Level after AGC
DIAG_MEM		7	R	NVRAM errors (Double bit-fails or CRC fail or shadow-register monitor failure)
DIAG_TEMP_HI		6	R	Temperature too high
DIAG_TEMP_LO		5	R	Temperature too low
DIAG_SPEED_HI		4	R	Magnet speed too high
DIAG_DSP_TA		3	R	DSP PLL lock error / Magnet acceleration error
DIAG_AGC_HI		2	R	Field too high/ AGC error
DIAG_AGC_LO		1	R	Field too low / AGC error
DIAG_DSP		0	R	Internal error

Please refer to the functional safety manual of the MLX90382.

7.1.1 Safe State 2 - SS2

Safe state 2 is issued on faults related to the NVRAM, **ER_NVM_DED** and **ER_NVM_CRC**, and shadow register, **ER_SR**, of the sensor.

In Safe State 2 all the sensor interfaces, except* SPI, are switched to tri-state (i.e. high impedance Hi-Z). This means that in conjunction with a pull-up resistor (R_PU) to VS placed at the corresponding ECU inputs, the sensor indicates a failure-band-high state. In conjunction with a pull-down resistor (R_PD) to GND placed at the corresponding ECU inputs, the sensor indicates a failure-band-low state.

* The SPI interface indicates the Safe State 2 as follows:

- If SS2 occurs and the **NV_SPI_FRCRCEN** is set, the reported CRC code is transmitted inverted.
- If SS2 occurs and the **NV_SPI_FRFSEN** is set, the Frame Start code FS is transmitted inverted.
- If SS2 occurs and the **NV_SPI_FRCRCEN** and **NV_SPI_FRFSEN** are NOT set, the sensor MISO returns to Hi-Z state after the FR command byte.

Read and write access to the NVRAM and shadow register remains possible during a Safe State 2 condition. If, for example, an **ER_CRC** error occurs after a :90382_SPI:NVm:Store instruction, an attempt can be made to correct the CRC by reinitiating a SPI_NvmUpdateCRC () cycle followed by a :90382_SPI:NVm:Store instruction.

Please refer to the functional safety manual of the MLX90382 for the explanation of the safety elements of the sensor.

Table 33: MCTRL Map – State register

Field	Address	Bit	R/W	Description
-		[15:8]	NU	Not used
STATE	44 0x002C	[7:0]	R	0x08: Norm state 0x10: Safe-State SS2 (NVRAM failure) 0x20: Safe-State SS2 0x40: Safe-State SS3

7.2 Digital Signal Processing

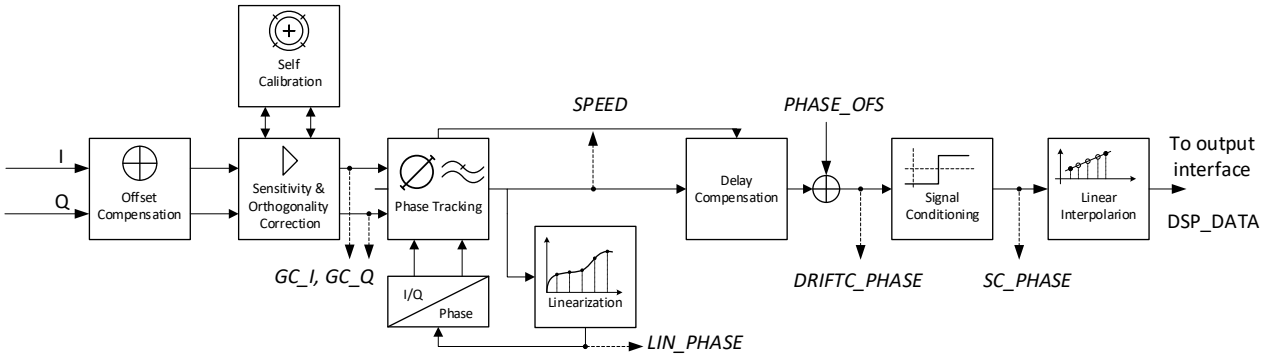

Figure 22: Digital signal processing architecture

Table 34: DSP register map

Field	Address	Bit	R/W	Description
AGC_GAIN	52 0x0034	[5:0]	R	Read current AGC gain setting
AGC_AMP	54 0x036	[12:0]	R	AGC measured amplitude
-		[15:13]	NU	Not used
TEMP	56 0x0038	[11:0]	R	Temperature according to SENT, range [200 : 0.125 : 711.875] [K]
-		[15:12]	NU	Not used
LIN_PHASE	58 0x003A	[15:0]	R	Angular value after linearization, resolution 360°/2^16.
SPEED	60 0x003C	[15:0]	R	v[Hz] = signed(SPEED_LO) / 2^22 * f_{AC}/26; v[rpm] = v[Hz] * 60; range ±6009,43
DRIFTC_PHASE	66 0x0042	[15:0]	R	Angular value after delay compensation and zero-point offset correction, resolution 360/2^16 deg.
SC_PHASE	68 0x0044	[15:0]	R	Angular value after signal conditioning
GC_I	72 0x0048	[15:0]	R	Gain-compensated I component (Averaging result)
GC_Q	78 0x004E	[15:0]	R	Gain-compensated Q component (Averaging result)
RMM_ASIQ	98 0x062	[15:0]	R	Adaptive orthogonality correction value AS_IQ
RMM_ASQQ	100 0x064	[15:0]	R	Adaptive sensitivity correction value AS_SQ

Definitions

The sensor has an automatic gain control on the gain stage in function of the applied magnetic field. The current gain setting can be read from the parameter **AGC_GAIN**. The gain range is limited by the parameters **AGC_GAIN_MIN** and **AGC_GAIN_MAX**, as explained in chapter “6.7 Gain configuration”. **AGC_AMP** represents the current AGC measured amplitude.

7.2.1 Angle measurements

The angle information is stored in 3 parameters in the DSP, each representing a stage in the DSP chain:

LIN_PHASE gives the angular position value after the *16-Point linearization*. The resolution of the value is 360°/2^16. **DRIFTC_PHASE** gives the angular position value after *Delay Compensation and Zero Position Adjustment*. The resolution of the value is 360°/2^16.
SC_PHASE gives the angular position value after *Signal conditioning.* The resolution is defined by the signal conditioning parameters SC_X1-2 and SC_Y1-2:

$$SC\_PHASE_{resolution} = (360°/2\text{^}16 * (SC\_X2 - SC\_X1))/(SC\_Y2 - SC\_Y1)\ [°/LSB]$$

SC_PHASE is the angle information reported on the outputs: SPI, SSI, PWM, ABI and UVW. For SPI the angle is reported with the FR command on FADDR0 by default, see chapter 6.5 SPI configuration.

7.2.2 Rotational speed measurement

The measured rotational speed (electrical), V_{el}, is a signed (2s-complement) 16-bit number represented by the concatenated register fields **DSP_SPEED**. V_{el} is calculated from the DSP_SPEED by the following formula:

$$V_{el}[Hz] = \frac{DSP\_SPEED[15:0] * f_{AC}}{2^{22} * 26}$$

Where:

$$f_{AC} = 20MHz$$

7.2.3 Main Clock Frequency f_{RCO} /ECU clock frequency synchronization on item level

As the DSP_SPEED measurement relates to the Application Clock Frequency f_{AC}, and thus the Main Clock Frequency, f_{RCO}. The measured V_{el} accuracy depends on the accuracy of the Main Clock Frequency, f_{RCO}.

At a Rotational Speed (electrical) V_{el} of +/-200krpm and a Main Clock Frequency inaccuracy of +/-5%, the absolute rotational speed inaccuracy would be +/- 10000 rpm. If the f_{RCO} frequency is lower than what is theoretically expected, the calculated speed will be higher than the actual speed.

To overcome this limitation a frequency synchronization on item level is proposed. This is supported by the sensor by a 16-bit rolling counter, **PWM_PCNT_ON** which can be read out via SPI. With ECU-defined time laps, e.g. 2ms, the **PWM_PCNT** can be compared to a corresponding ECU counter running in parallel.

E.g. if the 20MHz ECU counter would count within 2ms up to 2ms*20MHz=40000, a device with -5% frequency offset would return a **PWM_PCNT** difference of 2ms*20MHz*0.95=38000. The corrected speed estimate can then be computed as:

$$V_{el\_FEC}[Hz] = \frac{DSP\_SPEED[15:0] * f_{AC} * \Delta PCNT_{IC}}{2^{22} * 26 * \Delta PCNT_{ECU}}$$

Note that the **PWM_PCNT_ON** needs to be set to enable the **PWM_PCNT**, see PWM settings in Table 13.

Table 35: Register map – internal counter

Field	Address	Bit	R/W	Description
PWM_PCNT	260 0x0104	[15:0]	R	PWM period counter (PWM_PCNT_ON = 1)

7.2.4 I/Q measurements

GC_I and **GC_Q** give the averaging result of the gain-compensated I and Q component. The settings are controlled by the **DSP_IQNEG** and **DSP_GC_AVG** parameters. The parameters are signed 2's complement values.

From the **GC_I** and **GC_Q** signals, one can estimate the applied magnetic field with the following formulas. The formulas are valid for 35°C. To calculate the field, we need to know the sensitivity of the sensor. For this we need the IMC gain of the used application mode from Table 31, the gain configuration parameters **S_QQ and S_IQ** from the NVRAM and the current **AGC_GAIN** setting from the DSP register.

7.2.4.1 Gain/sensitivity calculation

$$SENSITIVITY\_35deg = 0.055\,V/V/T$$

$$GAIN = 32 * \left(3^{\frac{1}{16}}\right)^{AGC\_GAIN[5:0]}$$

Table 36: IMC gain per application mode

Parameter	Symbol	Typical	Magnetic Mode	Application Mode
IMC Gain for I-Channel	g_{IMC_I}	1.35	Rotary Mode (Mid Field)	X-Y, X-Z or Y-Z
		0.64	Rotary Mode (High Field)	X-Y, X-Z or Y-Z
		1	Stray-Field Immune Rotary Mode	X-Y
IMC Gain for Q-Channel	g_{IMC_Q}	1.35	Rotary Mode (Mid Field)	X-Y
		1.17	Rotary Mode (Mid Field)	X-Z or Y-Z
		0.64	Rotary Mode (High Field)	X-Y
		1.21	Rotary Mode (High Field)	X-Z or Y-Z
		1	Stray-Field Immune Rotary Mode	X-Y

7.2.4.2 Field estimation [T]

$$GC\_I[T] = \frac{int16(GC\_I[15:0]) + \frac{int16(SC\_IQ[15:0])}{2^{15}} * int16(GC\_Q[15:0])}{4 * 2^{14} * GAIN * g_{IMC\_I} * SENSITIVITY\_35deg}$$

$$GC\_Q[T] = \frac{int16(GC\_Q[15:0]) * \frac{2^{15}}{SC\_QQ[15:0]}}{4 * 2^{14} * GAIN * g_{IMC\_Q} * SENSITIVITY\_35deg}$$

7.2.4.3 Field estimation [T/mm]

$$GC\_I[T/mm] = \frac{2 * GC\_I[T]}{1.554mm}$$

$$GC\_Q[T/mm] = \frac{2 * GC\_Q[T]}{1.554mm}$$

7.2.4.4 Magnet properties

To have the optimum linearity with respect to a magnet position α, the signals B_1 and B_2 should be described as follows:

$$B_1 \div sin\,(90° - \alpha) \div cos\ \alpha$$
$$B_2 \div sin\ \alpha$$

In reality, the **magnetic field** at the **sensor's sensing element**, can be described according to the following formulas:

$$B_{1,A} = \left(90° - \alpha + \beta_{Magnet}\right)$$
$$B_1 = B_{1,O}(T) + B_{1,A}$$
$$B_{2,A} = (\alpha)$$
$$B_2 = B_{2,O}(T) + B_{2,A}$$

Where:
T is the temperature.
$B_{1,O}$ is the component B_1 offset (temperature dependent).
$B_{2,O}$ is the component B_2 offset (temperature dependent).
β_{Magnet} is the orthogonality error or phase error between the 2 components of the field.
$B_{1,A}$ is the component B_1 amplitude (temperature dependent).
$B_{2,A}$ is the component B_2 amplitude (temperature dependent).

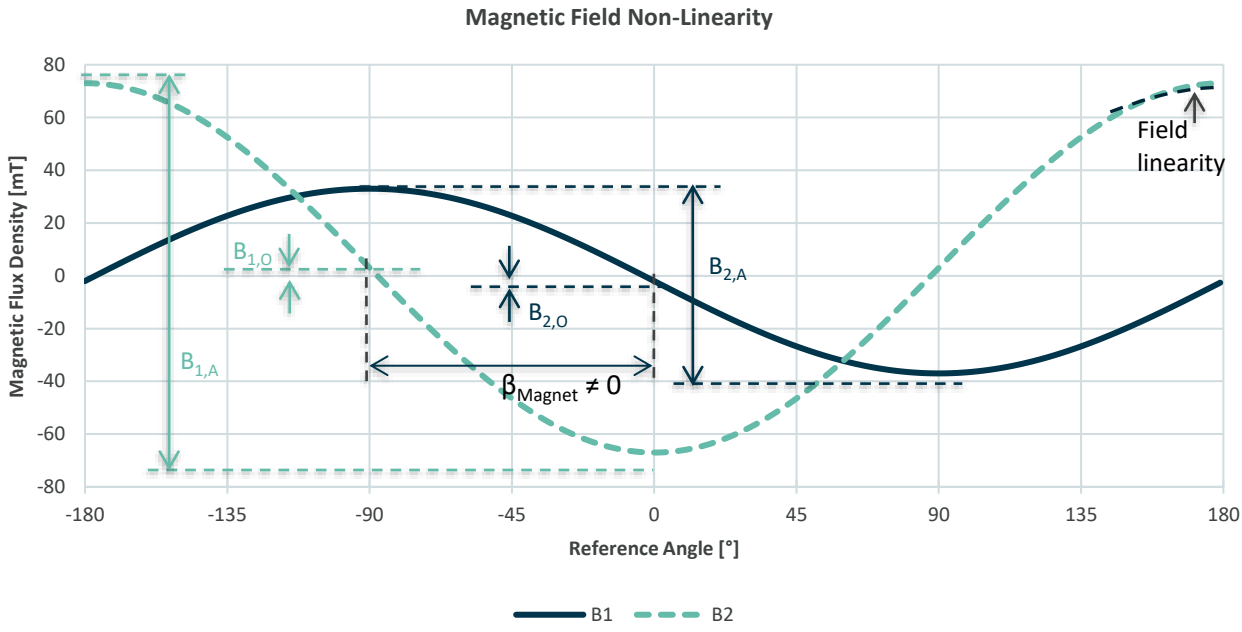

Figure 23: Non-ideal behaviours of the sine and cosine signals

The magnet imperfections can be compensated by the sensor as explained in this application note. But signal nonlinearity caused by saturation should be avoided.

7.2.4.5 Signal Nonlinearity

For the magnetic design, the magnetic mode of the sensor and the positioning of the sensor versus the magnet plays an important role. For a trough shaft and off-axis applications, the magnetization of the sensor has a higher impact on the signal nonlinearity than for End-of-shaft applications.
On sensor level there are two sources of signal nonlinearity:
Magnetic saturation if the applied field on the IMC location in X or Y direction is greater than 70mT or 160mT. In this case the air gap between the sensor and the magnet needs to be adapted;
Electrical saturation if the gain limits, **AGC_GAIN_MIN** and **AGC_GAIN_MAX,** of the sensor are set to high for the applied magnetics flux density. In this case the **AGC_GAIN_MIN** and **AGC_GAIN_MAX** need to be set open or adjusted to the applied magnetic field.

The signal non-linearity signature is easily recognizable: four periods over 360 degrees.

$$NLE_5 = a_5 \times sin\ (4 \times \alpha)$$

Figure **24** and Figure **25** illustrate an exaggerated electrical saturation of the input signals and the resulting angle nonlinearity.

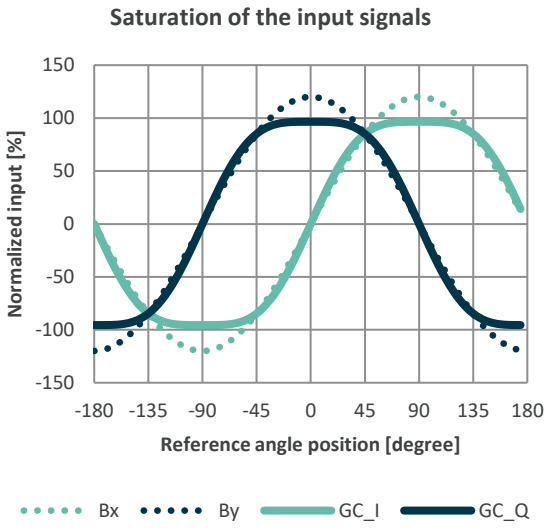

Figure 24: Electrical output signal saturation

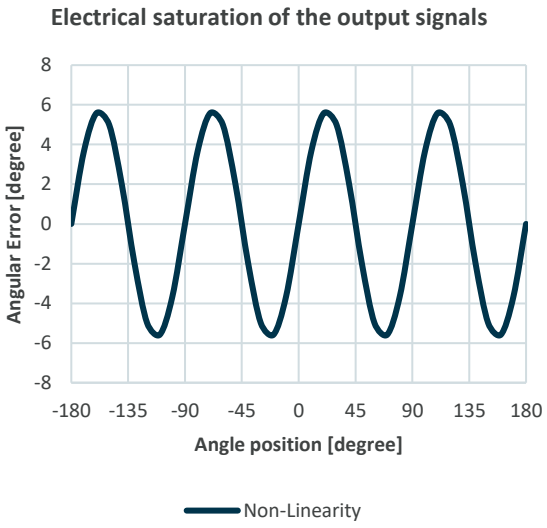

Figure 25: Angle nonlinearity due to signal saturation

7.2.4.6 Eddy Currents

For the PCB design of the MLX90382, one needs to be aware that a ground plain underneath the MLX90382 can cause Eddy Currents at high speed which disturbance appears mainly as a second-harmonic component of the angular error.

8 Glossary of terms & references

8.1 Glossary

Table 37: Glossary

Term	Description
ADC	Analog-to-Digital Converter
SR	Shadow Register
CRC	Cyclic Redundancy Check
DSP	Digital Signal Processing
EMC	Electro-Magnetic Compatibility
EoL	End of Line
NVRAM	Non-Volatile RAM
LSB/MSB	Least Significant Bit / Most Significant Bit
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
PWM	Pulse Width Modulation
Tesla (T)	SI derived unit for the magnetic flux density (Vs/m2)
ABI	Incremental encoder
GPIO	General Purpose Input / Output
f_{RCO}	Sensors Main Clock Frequency
f_{AC}	Sensors Application Clock Frequency
AGC	Automatic Gain Control
RMM	Residual Mismatch Measurement

9 Revision history

Table 38: Revision history

Revision	Date	Change history
001	December 2025	Release for MLX90382BAA

Tables

Figures

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